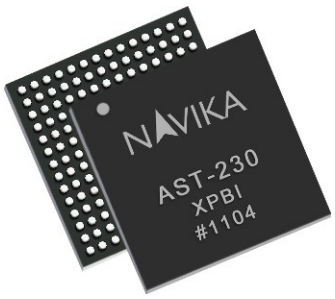
NAVIKA

AST-230: Application Processor with GPS Baseband

Features



AST-230

- 16-Channel high performance GPS-SBAS baseband
  - Indoor positioning
  - Fast time to fix
  - Integrated timing block
- ARM7 based processing engine
  - 90MHz operating frequency
  - JTAG and Trace support
  - ARM and Thumb mode
- Internal memory
  - 2Mbit SRAM
  - 32Kbit battery backed RAM
- Industry standard peripherals
  - USB 2.0 with Full Speed PHY
  - CAN 2.0 controller
  - SPI
  - TWI (I2C compatible)
  - Serial Port
  - UART
  - General Purpose I/O
- Low power mode
- Multiple boot mechanisms
- Scalable system clock frequency
- 3.3V I/O, 2.5V Core Supply voltage
- 12mm x 12mm BGA package
- Fully ROHS compliant

Product Description

AST-230 is a high performance GPS baseband with an ARM7 processing core and integrated peripherals.

The GPS baseband on the AST-230 provides 16 parallel acquisition and tracking channels and facilitates acquisition and tracking of very weak GPS signals. A large number of correlators enable very fast time to fix. In addition, a unique timing block for enhanced timing accuracy adds value to the AST-230.

AST-230 has the popular ARM7 core running at 90MHz. It supports both ARM and Thumb modes of operation and has JTAG interface for application development and debugging.

AST-230 is a peripheral-rich System-on-Chip. Several industry standard peripherals enable AST-230 to be used across segments. USB 2.0 full speed PHY support allows the AST-230 to be used for portable applications. CAN 2.0 controller has been integrated to support automotive applications. Other standard peripherals like UART, SPI, TWI and Serial Port provide varied communication interface options. Internal peripherals such as Timers, RTC, Battery backed counter and Watch dog timer provide several options for event based applications.

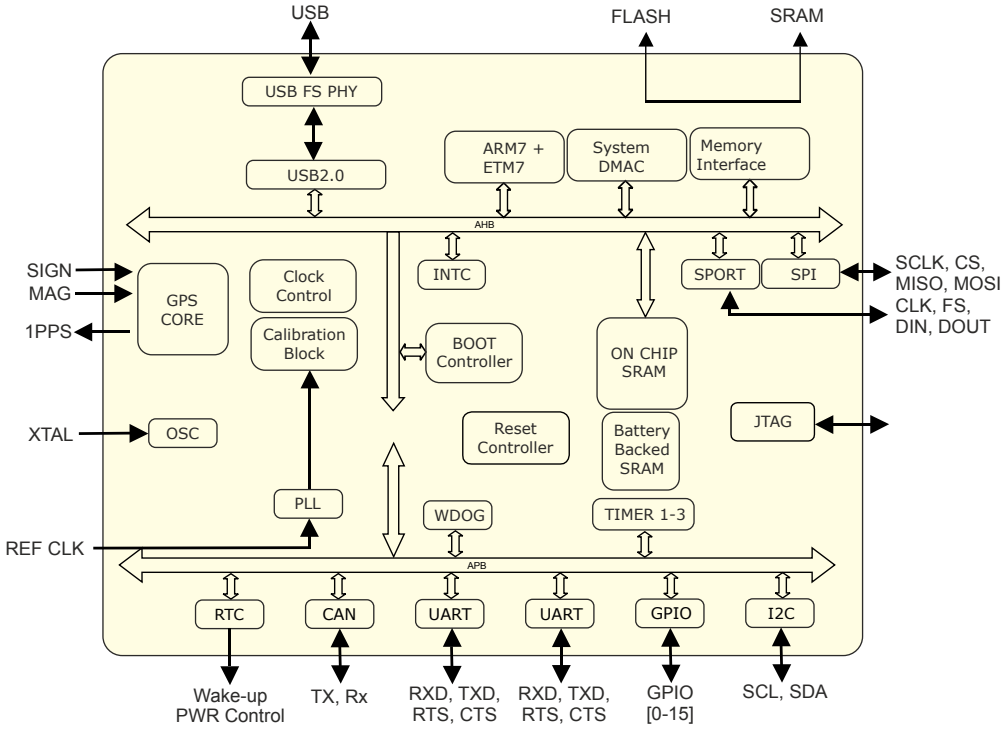
AST-230 supports an internal memory of 2Mbits that can be used to run application programs at the core frequency. In addition, 32Kbits of the memory is battery backed to facilitate retention of key configuration parameters.

AST-230 can be booted in multiple modes offering flexibility for system design. Application program can be stored either in parallel or serial flash or can be loaded from a SPI master.

The operating frequency of AST-230 can be programmed to operate at different frequencies upto a maximum of 90MHz. The flexible scaling offers an option to the application program to trade the operating speed and power consumption.

For power sensitive applications, AST-230 has a low power mode that can reduce the overall power dissipation of the system.

A typical block diagram of the AST-230 is shown below



The different blocks of the AST-230 are interconnected through AMBA standard AHB or APB buses. The AHB bus can operate at a maximum of (core / 2) Hz while the APB works at a maximum of (AHB / 2) Hz.

ARM7 core of the AST-230 is associated with an Interrupt controller and a DMA controller. Further, the Memory controller allows the AST-230 to be interfaced with synchronous or asynchronous memories. The external bus interface can address upto 32Mbits of memory space.

AST-230 has multiple power domains. It operates on a core voltage of 1.2V and can work from either 2.5V or 3.3V I/O voltage. In addition, the battery domain requires 1.2V.

The AST-230 is packaged in a 12mm x 12mm FBGA package with 196 functional and power supply pins. It supports industrial temperature range of -40 ^{0}C to +85 ^{0}C.

Specifications of AST-230

GPS Baseband

Acquisition Channels	:16
Tracking Channels	:16
Acquisition Sensitivity	:-160 dBm
Tracking Sensitivity	:-163 dBm
GPS power consumption	: 50 mW (Tracking)
RF Interface	:2-bit; SIGN, MAG
GPS Sampling Clock	:16.368MHz

PROCESSING CORE – ARM7

Operating frequency	:90 MHZ
Bus architecture	:AMBA Standard – AHB and APB
AHB frequency	:45 MHZ (max)
APB frequency	:22.5 MHz (max)
Instruction set	:ARM and Thumb modes

USB

PHY	:Full speed
Communication Interface	:VCC, GND, D+, D-

CAN

Specification	:CAN 2.0
Mailboxes	:16 for objects of 8-bytes data length, 4 Transmit-only, 4 Receive-only, 8 Transmit-Receive
Remote frames	:Extended data and remote frame support
Communication Interface	:CAN Tx and Rx

SPI

System Clock	:22.5 MHz (max)
Slave select	:6
Chip select	:1
Modes	:Master, Slave, Multi-master, Boot
Interrupt	:Supported
DMA	:Supported

TWO WIRE INTERFACE (TWI)

System Clock	:400 Khz
Modes	:Master, Slave, Multi-master
Function Select	:Selection between GLONASS or GPS / QZSS functionality
Interrupt	:Supported

SERIAL PORT (SPORT)

System Clock	:22.5 MHz
Clock source	:Internally generated or External source
Word length	:3 to 32 bits, big or little endian
Framing	:Supported
Interrupt	:Supported
I2S	:Supported
Multi-channel capability	:Supported

UART

Speed of operation	:Up to 1 Mbps
Type	:Full UART with frame control
Word length	:7 to 12 bits
Interrupt	:Supported
DMA	:Supported

GPIO

Available ports	:16 bi-directional; configurable as either input or output
Interrupt	:Supported

TIMER

Available	:3
External clock input	:Supported
Interrupt	:Supported

REAL TIME CLOCK (RTC)

Mode	:32-bit free running counter
Clock	:32.768 KHz crystal
Power down / wake up features	:Supported

WATCH DOG TIMER (WDT)

Mode	:32-bit counter; programmable through software
Clock	:32.768 KHz crystal
Configuration	:Core and Peripheral reset upon expiry of counter
Traceability	:Sticky bit to indicate if reset happened due to Watch Dog function

CLOCKS

System Clock	:90 MHZ (max)
Peripheral Clock	:45 MHZ (max)
Battery backed peripherals	:32.768 Khz

RESET

Reset	:Active Low Chip Reset, at least 25 ms low pulseResets the entire chip
GPS_Reset	:Active low Reset, at least 3 clocks wideResets the GPS correlator only

JTAG

JTAG	:TDO, TDI, TCK, TMS and TRST lines

POWER SUPPLY

Core Supply	:1.2 V
I/O Supply	:2.5 V / 3.3 V
Battery Supply	:1.2 V

PACKAGING

Type	:FBGA
Balls	:196, 0.8 mm pitch

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