NAVIKA

AST-234

Integrated GPS Baseband Chip

FEATURES

- High performance GPS Baseband
- 8K GPS correlator architecture for enhanced sensitivity and faster time to first fix
- Indoor positioning capability with sensitivity of –163dBm
- Lightning fast positioning with fix times of less than a second
- Accurate time output
- ARM7 based processing engine with upto 90MHz clock speed
- Internal high speed SRAM of 2Mbits and 32Kbits of battery backed SRAM to store configuration parameters
- On-chip industry standard peripherals such as USB 2.0, CAN 2.0, Serial Port, SPI, TWI, UART, GPIO
- Supports low power modes supported by wakeup from system RTC
- Multiple boot mechanisms for desired system configuration
- Scalable system clock frequency to suit processing requirements

PERIPHERALS

- USB 2.0 Device with FULL SPEED support
- Two UART interfaces
- 9 bi-directional GPIOs
- Two Wire Interface (TWI) (I2C compatible)
- SPI
- SPORT
- CAN Controller
- Three Timers
- RTC and Watchdog timers
- ETM7 provides CPU trace and debug support
- JTAG and Multiplexed trace ports – 8 bit trace

APPLICATIONS

AST-234 is a miniature version of the AST-230 SoC from Navika Electronics. It is a low cost platform for wide variety of applications, which involves GPS and other peripherals.

The main segments where AST-234 is an ideal choice is

- GPS modules
- Base station timing Solutions
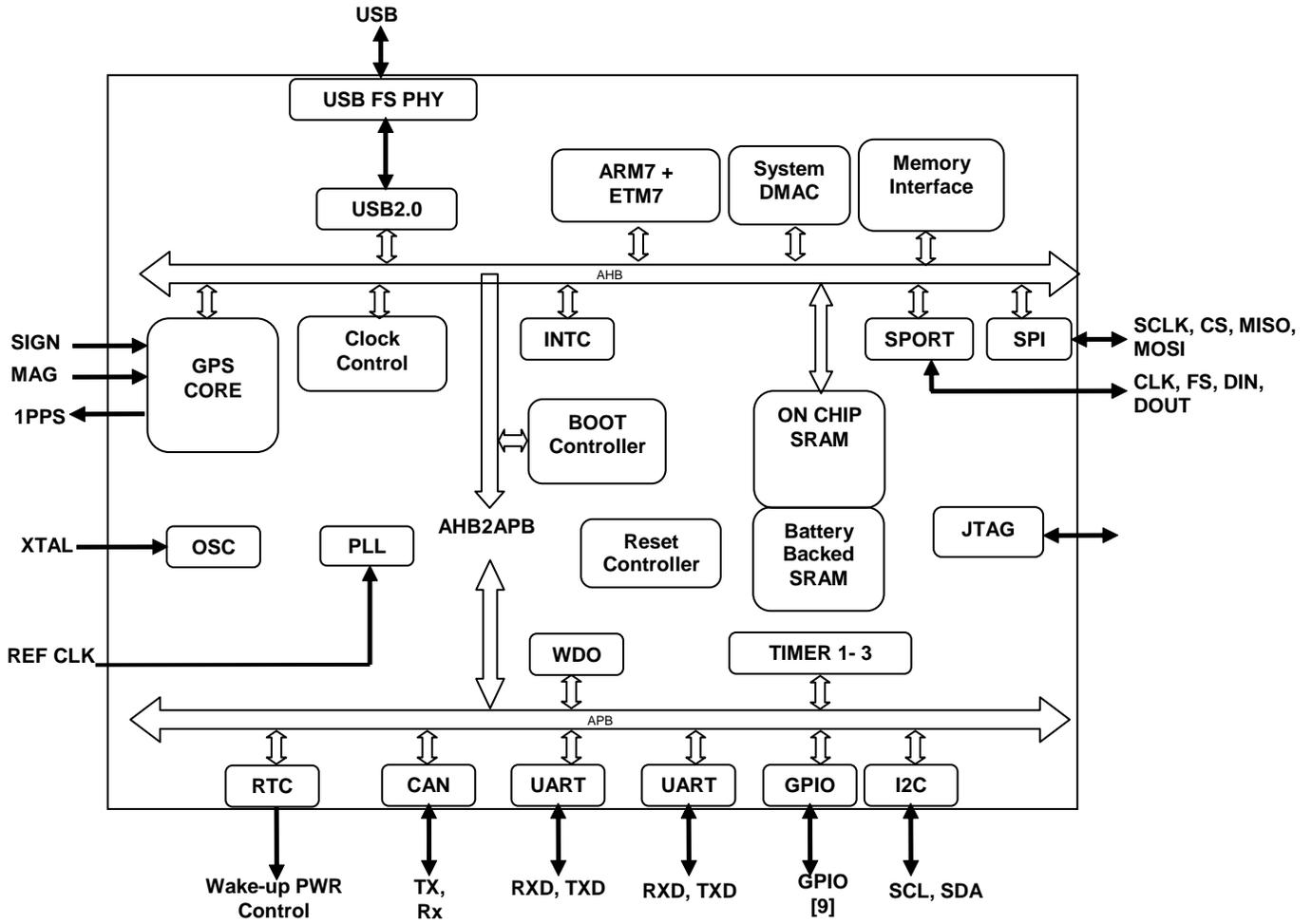- Automotive applications

FUNCTIONAL BLOCK DIAGRAM

Figure 1: Block Diagram of AST-234

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REVISION HISTORY

March 2015-Revision 1.01

GENERAL DESCRIPTION

AST-234 is a high performance GPS baseband System on Chip aimed at diverse applications in Automotive, Consumer Electronics, Infrastructure, Healthcare and Industrial market segments.

In addition to the GPS baseband, the AST-234 has the highly popular ARM7 processing core along with a host of rich peripherals and on-chip memory to support not just stand-alone functions but also applications combining several functionalities.

The AST-234 also combines several core building blocks such as PLL, Memory Controller, Boot Controller, Reset Controller and 32.768KHz Oscillator to facilitate simpler system integration.

GPS BASEBAND

At the heart of the AST-234 is the GPS baseband. This is a 16-channel correlator capable of interfacing with a standard GPS front-end and processing the GPS signals. The in-built correlators are designed to provide the maximum sensitivity and the shortest time to acquisition, thereby ensuring that the chip delivers unmatched performance. The GPS baseband is seamlessly connected to the ARM7 processing core through the AHB bus to exchange the programming parameters and the correlation results. The GPS firmware running on the ARM7 processing core runs the tracking loops and navigation algorithms using a small memory and MIPS footprint.

The GPS core also integrates a 48-bit counter, which runs over the battery power and is clocked by the 32.768KHz oscillator block. The counter is used to maintain precise time to facilitate a fast time to first fix from the GPS core.

The GPS core can be reset by two means –

➢ Asserting the master reset MRESET_N low for about 2msec
➢ Asserting the GPS Correlator reset GPS_RESET_N low for about 2msec

ARM7 PROCESSING CORE

AST-234 contains an ARM7TDMI processing core. The core consists of 16 general-purpose registers of 32-bit width. The ARM7 core is interfaced to several functional blocks such as Interrupt Controller, Memory Controller and DMA Controller to form a complete processing sub-system.

The ARM7TDMI process operates in two modes –

ARM mode: 32-bit word aligned instructions executed in this mode.
Thumb Mode: 16-bit, half-word aligned Thumb instructions executed in this mode.

MEMORY ARCHITECTURE

AST-234 views memory as a single unified 4G-byte address space that can be accessed using 32-bit addressing. All resources, including internal memory, external memory, and I/O control registers occupy separate sections of this common address space.

AST-234 has 2Mbits [256Kbytes] of internal SRAM, of which 32Kbits [4Kbytes] are battery backed up, to store system parameters and GPS data.

The Peripheral DMA controller provides high-bandwidth data movement capability. It can perform block transfers of code or data between the internal memory and peripheral or vice versa or Peripheral to external memory.

LOW POWER ARCHITECTURE

AST-234 provides power saving options by providing frequency scaling through user control. It employs two power supply domains and ensures that the critical information is retained in the chip through the battery power even when the main power is turned OFF.

SYSTEM INTEGRATION

AST-234 is a highly integrated System on Chip. In addition to the GPS baseband and a host of peripherals, AST-234 also contains the crucial blocks required for system integration. These are described below.

RTC OSCILLATOR

AST-234 integrates a 32.768KHz oscillator, which is useful to drive an internal Real Time Clock and a battery-backed counter. The oscillator can be driven by a standard crystal of 32.768KHz and is powered from the battery domain.

SYSTEM BUSES

The AST-234 system has two system buses – AHB [ARM AMBA Advanced High Performance Bus], where all the main blocks requiring relatively higher bandwidth are placed and APB [ARM AMBA Advanced Peripheral Bus] where all the low bandwidth peripherals are placed.

CLOCK CONTROL

AST-234 derives all the required internal clocks from an external clock of 16.368MHz. An internal PLL derives a higher system frequency [PLL_CLOCK] of 180.048MHz through which the clocks required by various blocks are derived. The default configuration ensures that the AHB frequency is kept at 90 MHz.

RESET CONTROLLER

AST-234 has an in-built reset controller that generates an active low reset pulse for all internal blocks. The reset controller takes inputs from different sources such as power OFF-ON cycle, watchdog timer expiry and software reset and delivers a single reset pulse. The trigger to the reset controller can be the output of a reset generator external to the AST-234 or a simple RC network.

AST-234 PERIPHERALS

AST-234 contains a rich set of peripherals connected to the core via high bandwidth buses (AHB and APB), providing flexibility in system configuration as well as excellent overall system performance (see Figure 1). The AST-234 processor contains dedicated serial communications ports (SPI, SPORT, TWI and UART) and an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

USB CORE

AST-234 provides a full speed USB 2.0 controller to support direct connection to a host system at 12M bits per second data rate. The interface provides a flexible programmable environment with up to seven data end points and one control endpoint. Each endpoint can support all of the USB data types and packet sizes including control, bulk, interrupt, and isochronous. When AST-234 is operating as a USB device, it is capable of bus-powered operations. To accomplish this, the USB device must be capable of operations when the core clock and system clock are running at the same frequency as the USB full speed input (60 MHz). This ensures that the AST-234 can run at lowest current until it can request more current from the host. The AST-234 USB controller has dedicated DMA channels and interrupts completion channels to minimize processor polling overhead and to enable asynchronous requests for CPU attention only when transfer management is required.

SPI – SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) is an industry standard synchronous serial link designed to communicate with multiple SPI-compatible devices.

SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full duplex, synchronous serial interface, which supports both master and slave modes and can operate in a multi-master environment. This peripheral implementation includes programmable baud rates, clock phase and clock polarity. The SPI is essentially a shift register that serially transmits and receives data bits to/from other SPI devices. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines.

The SPI block is configured in SLAVE mode by default (after reset). The major applications of SPI in AST-234 are

- Load the boot image by an external host when host boot option is selected
- Load the boot image from an external serial flash when external flash boot option is selected
- As a serial interface for data transfer between SPI-compatible devices

SPORT

AST-234 incorporates one dual-channel synchronous Serial Port (SPORT) for serial and multiprocessor communications.

The SPORT supports the following features:

- Bi-directional operation – The SPORT has independent transmit and receive pins, enabling eight channels of I2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking –The transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (fSCLK/131,070) Hz to (fSCLK/2) Hz.
- Word length –The SPORT supports serial data words from 3 to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – The transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Interrupts – The transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multi-channel capability – The SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

UARTS

AST-234 integrates one full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity.

The UART port supports following two modes of operation:

PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.

DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

> Supports bit rates ranging from (fSCLK/1,048,576) to (fSCLK/16) bits per second
> Supports data formats from seven to 12 bits per frame
> Both transmit and receive operations can be configured to generate maskable interrupts to the processor

RTC AND WAKEUP TIMER
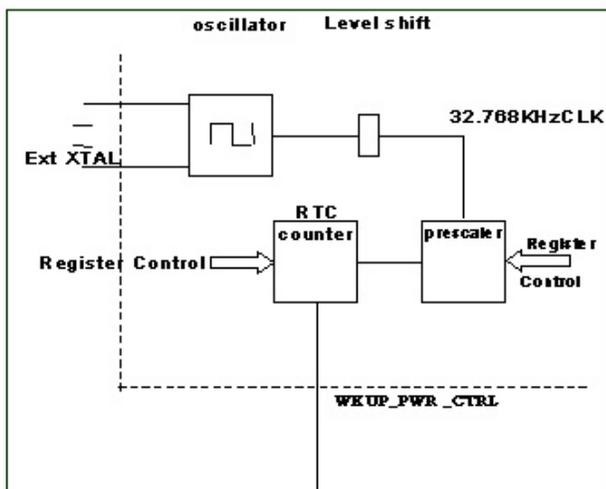
The Real Time Clock (RTC) provides counters, which gives the real time. The RTC is clocked by a 32.768 kHz crystal external to the AST-234. The RTC Oscillator on-chip generates the required clock frequency output to drive the RTC. The RTC block is powered up by battery backup and clocked even when the rest of the processor is in a low-power state. The RTC contains a 32-bit free running counter, which is clocked by 1Hz signal. It counts up from the initial value of 0x0000000 up to 0xFFFFFFFF and then rolls over to 0x00000000, incrementing by 1 each time a 1Hz tick is seen.

The 32.768 kHz input clock frequency is divided down to a 1Hz signal by a pre-scaler.

The RTC also provides the functionality of a wakeup timer, programming which it is possible to generate events at specified time, which can be used to power down or power up the system.

WATCHDOG TIMER

The watchdog module provides a way of recovery from software crashes. The watchdog clock is used to generate regular interrupt, depending on a programmed value. The watchdog monitors the interrupt and asserts a reset signal if the interrupt remains un-serviced for the entire programmed period. The watchdog can be enabled or disabled as required.

AST-234 includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

The watchdog timer resets both the core and the AST-234 peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

TIMERS

There are three general-purpose programmable timer units in AST-234. These timers can be synchronized to an external clock or to the internal clock. The external timer clock should less than APB clock. The timer units can be used in conjunction with the two UART's to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels. The timers can generate interrupts to the processor core providing periodic events for synchronization.

Any of these three timers can be clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

TWO WIRE INTERFACE

AST-234 includes a two-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I2C™ bus standard. The TWI module offers the capabilities of master and slave operation support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The default Master/Slave address is 0x00.

The TWI incorporates the following features:
- Simultaneous Master and Slave operation on multiple device systems
- Support of multi master data arbitration
- 7 and 10 bit addressing
- 100 kbits/s and 400 kbits/s data rates
- General Call Address support
- Master Clock synchronization and support for clock low extension
- Separate multiple byte receive and transmit fifo's
- Low interrupt rate
- Individual override control of data and clock lines in the event of bus lock-up
- Single interrupt output request line

GPIO

AST-234 has 9 bi-directional, general-purpose I/O (GPIO) pins allocated across two separate GPIO modules. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers. The GPIO module is connected as a peripheral through APB bus. The GPIO's can be controlled in two modes.

- Software mode through APB interface
- Hardware mode, through a hardware control interface

The CPU controls the accesses to the data, control and status information of the GPIO through the APB bus interface. When the software control mode is enabled, the data direction register controls the direction of data transfer. When hardware mode is enabled, data direction is controlled through the auxiliary port direction control pins. Similarly, data written and read through this port, but pin status can also be read through the APB interface. The default state of the pins is input.

CAN CONTROLLER

The CAN protocol is an ISO standard (ISO 11898) for serial data communication. The protocol is meant for the automotive applications. CAN protocol has gained widespread use in industrial automation as well.

The interface to the CAN bus is a simple two-wire line. This means, there is an input pin Rx and an output pin Tx. Both pins operate with TTL level and are appropriate for the operation with CAN bus transceivers according to ISO/DIS 11898 or with a modified RS-485 interface.

In the standard implementation, 3 acceptance mask registers and 16 mailboxes are implemented.

The standard features supported by the CAN controller are listed below

- Supports CAN specification 2.0B (active)

- Base data and remote frames
- Extended data and remote frames
- 16 mailboxes for objects of 8-bytes data length
- 4 transmit only mailboxes (mailbox 15 to 12)
- 8 transmit/receive mailboxes (mailbox 11 to 4)
- 4 receive only mailboxes (mailbox 3 to 0)
- One programmable global mask for Message Objects 4 to 11
- Two programmable local masks for Message Objects 0/1 and 2/3
- Acceptance mask register for identifier extension bit
- Receive Message Overwrite Protection
- Priority logic for Transmit Message Objects (Priority defined by mailbox number
- Single Shot Transmission
- Flexible Remote Frame Handling
- Programmable bit rate
- Flexible interrupt structure
- Flexible status interface
- Self Test Mode (Loop back on CAN bus)
- Readable error counters. Write access to the CAN error counters (for test purposes)
- 8/16 bit CPU Interface - No wait states (minimum length of CPU signals is required)

BOOTING

AST-234 has two mechanisms for loading the internal memory after reset. The BOOT_MODE pins govern the boot mechanism in AST-234.

- When BOOT_MODE [1:0] = '00': In this case an external host can download the boot image into internal memory via SPI interface. Here the AST-234 acts as SPI slave
- When BOOT_MODE [1:0] = '01': In this case an AST-234 can download the boot image from external SPI flash into internal memory via SPI interface. Here the AST-234 acts as SPI master

In all the modes, there is an option for the software to initiate memory BIST before actually downloading the image. The boot loader is supposed to check the status of memory BIST and repair before actually downloading the image.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter	Conditions	Min	Nominal	Max	Units
Internal Supply Voltage		1.08	1.2	1.32	Volts
External Supply Voltage	$VIH = 1.7V$, $VIH_{clock} = 1.9V$	2.25	2.5	2.75	Volts
	$VIH = 2.2V$, $VIH_{clock} = 2.4V$	2.7	3.0	3.3	
32KHz OSC Supply Voltage		1.08	1.2	1.32	Volts
PLL Supply Voltage		1.08	1.2	1.32	Volts
USB Core Supply		1.08	1.2	1.32	Volts
USB IO Supply		3	3.2	3.3	Volts
High Level Input Voltage (VIH)		1.6		2.8	Volts
Low Level Input Voltage (VIL)		-0.3		+0.7	Volts
Junction Temperature (Tj)		-40	+25	+85	C
High Level output Voltage (VOH)		1.7	1.8		Volts
Low Level output Voltage (VOL)			0.2	0.7	Volts
High Level output Current (IOH) @ VOH 1.7 V		7.5	12.3	18.2	mA
High Level output Current (IOH) @ VOL 0.7 V		5.8	9.3	12.9	mA

Table 1: Operating Conditions

ELECTRICAL CHARACERISTICS

Parameter	Test Conditions	Min	Typical	Max	Unit
High Level output Voltage (VOH) @IOH 4mA		1.7			Volts
Low Level output Voltage (VOL) @IOH 4mA		0.7			Volts
High Level output Current (IOH) @ VOH 1.7 V		7.5	12.3	18.2	mA
High Level output Current (IOH) @ VOL 0.7 V		5.8	9.3	12.9	mA
Input capacitance 1) CLK_Ref 2) SCLK 3) SIGN, MAG (GPS) 4) SDIN, RFS, TFS 5) SPORT Output capacitance 1) PTTI (GPS) 2) Other GPS Ports 3) BBC_INT_B 4) SPORT (ARM) 5) SDOUT		5 10 5 10 10 20 15 15 15 15			pf

Table 2: Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Rating

Parameter	Rating
Internal Supply Voltage	1.32 V
External I/O Supply voltage	3.6 V
Input Voltage 1	-0.3 to 0.7 V
Input Voltage 2	1.7 to 2.8 V
Output Voltage Swing	0 to 3.3 V
Load Capacitance	20 pf
Storage temperature range	-65 ^{0}C to 150 ^{0}C
Junction Temperature Under bias	-40 ^{0}C to 85 ^{0}C

Table 3: Absolute Maximum Rating

ESD SENSITIVITY
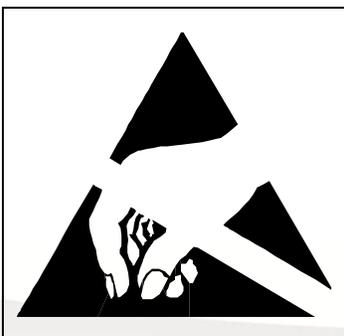
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AST-234 pin definitions are listed in Table 16.

Functional Pin Description

Port Name	Description	Default Value	Pull Up / Pull Down	I/O
REF_CLK	16.368Mhz Clock as PLL Input Clock and Reference Clock for GPS core		NA	I
SPORT_XCLK	SPORT X Channel Clock		PD	I/O
SPI_CLK	Serial Port Interface Clock		NA	I/O
MRESET_N	Active Low Asynchronous Master Reset Input		NA	I
GPS_RESET_N	External Asynchronous active low Reset Input for GPS Correlator		PU	I
SPI_FLASH_CS	SPI Flash Chip Select	Z	NA	O
BOOT_MODE_0 BOOT_MODE_1	Boot Mode Selection. 00: Booting through SPI host 01: Booting through SPI Flash 10: Not used 11: Not used		NA	I
VDD_ISO_ENABLE	Active Low Signal Indicating VDD is OFF.		PU, PD	I
UART1_TX	UART1 Transmit Output Signal	HIGH	NA	O
UART1_RX	UART1 Receive input Signal		NA	I
UART2_TX	UART2 Transmit Output Signal	HIGH	NA	O
UART2_RX	UART2 Receive input Signal		PU	I
SIGN	Bit 1 of IF sample from the GPS RF. When using AST-GPSRF, this is driven by the AST-GPSRF on the rising edge of REF_CLK.		NA	I
MAGN	Bit 0 of IF sample from the GPS RF. When using AST-GPSRF, this is driven by the AST-GPSRF on the rising edge of REF_CLK		NA	I
PTTI	Precise One second pulse from GPS core	LOW	NA	O
GPS_INT	10ms Interrupt to the processor	LOW	NA	O
GPIO0	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO1	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO2	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO3	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO4	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO8	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO9	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO10	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO11	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
SPI_MOSI	SPI Master Output		NA	I/O
	SPI Slave Input	Z		I/O
SPI_MISO	SPI Master Input		NA	I/O
	SPI Slave Output	X		I/O
SPI_CS	SPI Chip Select	Z	NA	I/O
SPORT_XFS	Frame sync (internally tied to YFS)	Z	PD	I/O
SPORT_XADATA	SPORT X channel A data	Z	PD	I/O
SPORT_YADATA	SPORT Y channel A data	Z	PD	I/O
TWI_SCL	TWI (I2C compatible) Serial Clock Data	HIGH	NA	I/O
TWI_SDA	TWI (I2C compatible) Data Pin	HIGH	NA	I/O
CAN_TX	CAN Controller TX Data Output	HIGH	NA	O
CANC_RX	CAN Controller Receive Data Input		PD	I

nTRST	JTAG Reset Input			PU	I
TCK	JTAG Clock Input			NA	I
TDI	JTAG Data Input			PU	I
TDO	JTAG Data Output	Z		NA	O
TMS	JTAG MODE Select Input			PU	I
USB_DP	USB D+ line to the PHY			NA	I/O
USB_DM	USB D- line to the PHY			NA	I/O
USB_VBUS	VBUS Input pin			NA	I/O
XIN	Crystal signal input for RTC, 32.768KHz			NA	I
XOUT	Crystal signal output for RTC, 32.768KHz			NA	O

Table 4: Functional Pin Description

TIMING SPECIFICATIONS

Table describes the timing requirements for the signals used in AST-234 chip. All the peripheral interface timing is also shown below.
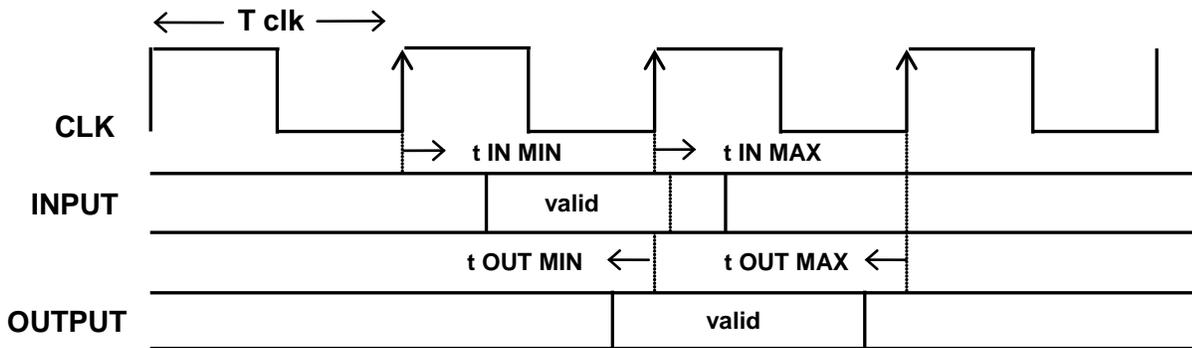

Figure 2: Min and Max Delays with respect to clock

GPS Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
GPS_SIGN	1	20	-	-
GPS_MAG	1	20	-	-
BBC_INT_B	-	-	0	25
tCLK (clk_ref)	16.368MHz			
tCLK (GPS_SYS_CLK)	72MHz			
tCLK (SCLK)	21MHz			

Table 5: GPS Signals

GPIO Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
GPIO	3	10	1.5	6
tCLK (PCLK)	45Mhz			

Table 6: GPIO Signals

SPI Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
MOSI	1.6	18.4	1	14
MISO	-1.5	9.5	0	10
SPI_CS	1.5	10	-	-
SPI_FLSH_CS	1.5	10	-	-
tCLK	22.5MHz			

Table 7: SPI Signals

SPORT Signals

Signals (For both Channels)	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
SPORT_XDATA	1	10	0	3
SPORT_XFS	1	10	0	3
SPORT_YDATA	1	10	0	3
SPORT_YFS	1	10	0	3
tCLK	22.5MHz			

Table 8: SPORT Signals

Serial Interface Signals to PCM Codec

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
CIF_SDIN	18	18	-	-
CIF_SDOUT (w.r. to -ve edge of	-	-	13.89	8
CIF_FS (w.r. to -ve edge of cif_bclk clock)	-	-	13.89	8
tCLK	25MHz			

Table 9: Serial Interface Signals to PCM Codec

CAN Controller Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
CANC_TX	-	-	2	6
CANC_RX	3	10	-	-
tCLK (PCLK)	45 MHz			

Table 10: CAN Controller Signals

JTAG Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
TDI	2	12	-	-
TDO	-	-	2	6
TMS	2	12	-	-
tCLK	25 MHz			

Table 11: JTAG Signals

Clock and Reset Timing

Parameter	Minimum	Maximum	Unit
Timing Requirements			ns ns ns ns ns
tCKIN CLKIN Period tCKINL CLKIN Low Pulse tCKINH CLKIN High Pulse tWRST RESET Asserted Pulse Width Low	62 31 31 TBD		

Table 12: Clock and Reset Timing

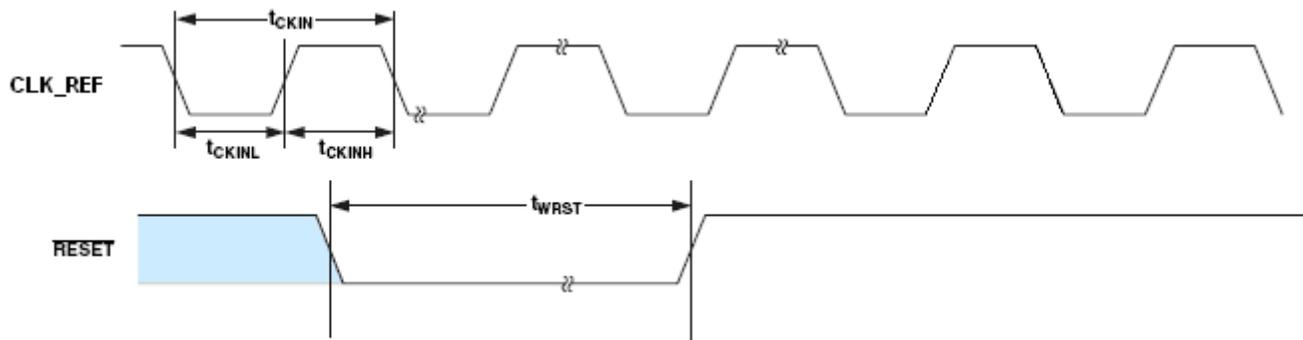**Clock and Reset Timing**

Figure 3: Clock and Reset Timing

Serial Peripheral Interface (SPI) Port—Master Timing
The below table and figure describes SPI port master operations.

Serial Peripheral Interface (SPI) Port—Master Timing

Parameter	$V_{DDEXT} = 1.8\,V$ LQFP/PBGA Packages		$V_{DDEXT} = 1.8\,V$ MBGA Package		$V_{DDEXT} = 2.5\,V/3.3\,V$ All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{SSPIDM} Data Input Valid to SCK Edge (Data Input Setup)	10.5		8.5		7.5		ns
t_{HSPIDM} SCK Sampling Edge to Data Input Invalid	−1.5		−1.5		−1.5		ns
Switching Characteristics							
t_{SDSCIM} $\overline{SPISELx}$ Low to First SCK Edge	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICHM} Serial Clock High Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLM} Serial Clock Low Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLK} Serial Clock Period	$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		ns
t_{HDSM} Last SCK Edge to $\overline{SPISELx}$ High	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPITDM} Sequential Transfer Delay	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
$t_{DDSPIDM}$ SCK Edge to Data Out Valid (Data Out Delay)	0	6	0	6	0	6	ns
$t_{HDSPIDM}$ SCK Edge to Data Out Invalid (Data Out Hold)	−1.0	+4.0	−1.0	+4.0	−1.0	+4.0	ns

Table 13: Serial Peripheral Interface (SPI) Port—Master Timing

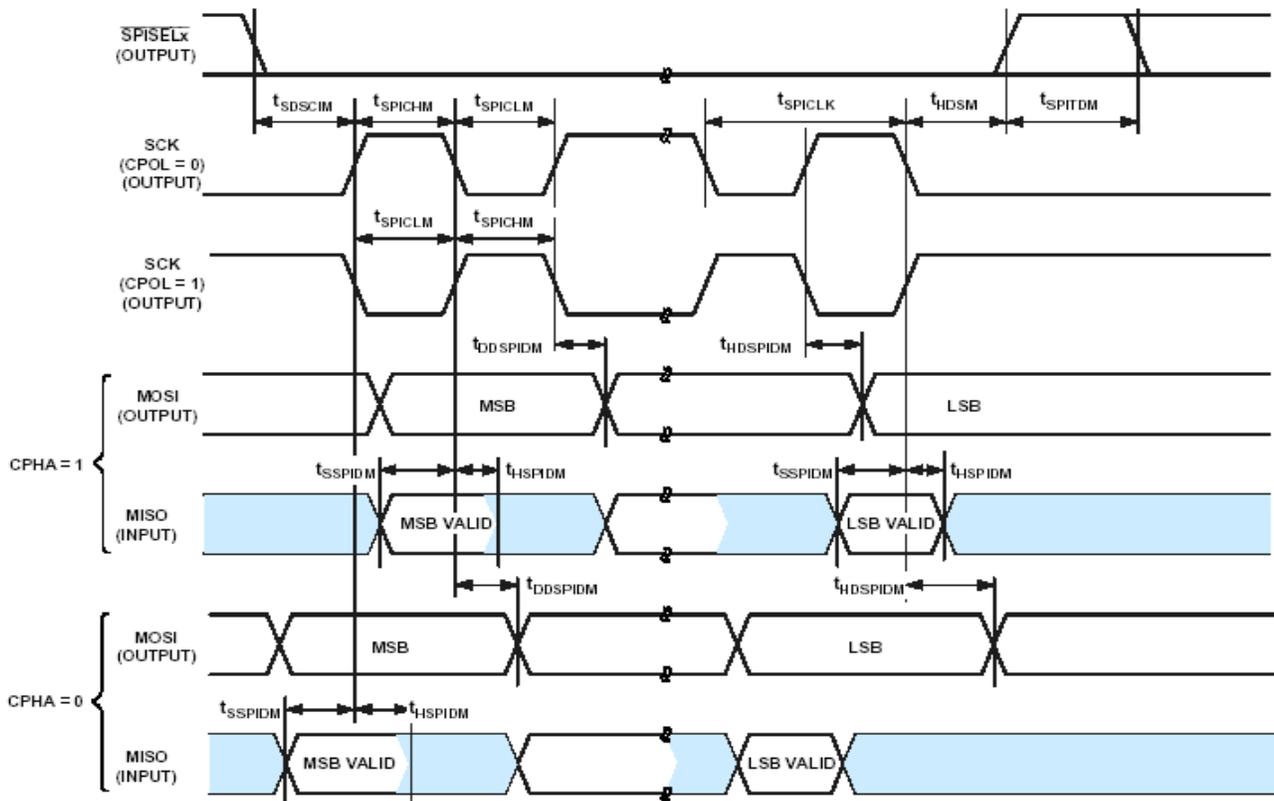## Serial Peripheral Interface (SPI) Port—Master Timing

Figure 4: *Serial Peripheral Interface (SPI) Port—Master Timing*

Serial Peripheral Interface (SPI) Port—Slave Timing
Below Table and Figure, describe SPI port slave operations.

Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V MBGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		Unit
	Min	Max	Min	Max	Min	Max	
Timing Requirements							
t_{SPICHS} Serial Clock High Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLS} Serial Clock Low Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLK} Serial Clock Period	$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		ns
t_{HDS} Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPITDS} Sequential Transfer Delay	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SDSCI} $\overline{SPISS}$ Assertion to First SCK Edge	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SSPID} Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID} SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics							
t_{DSOE} $\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI} $\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID} SCK Edge to Data Out Valid (Data Out Delay)	0	10	0	10	0	10	ns
t_{HDSPID} SCK Edge to Data Out Invalid (Data Out Hold)	0	10	0	10	0	10	ns

Table 14: Serial Peripheral Interface (SPI) Port—Slave Timing

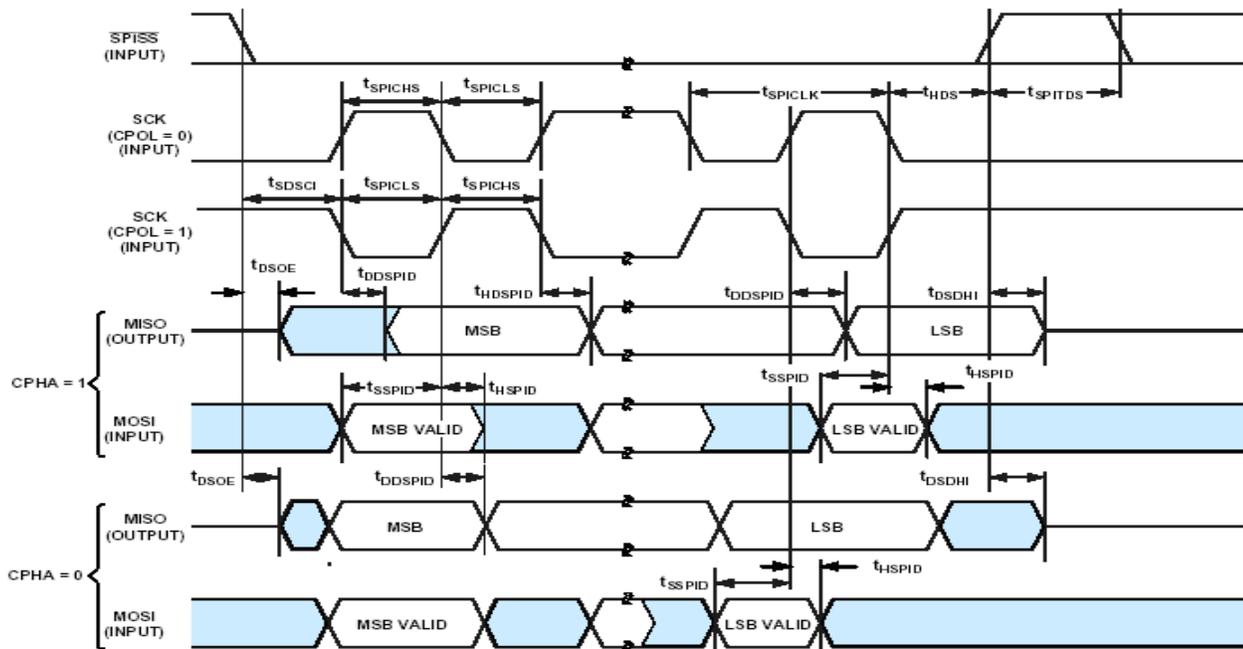## Serial Peripheral Interface (SPI) Port—Slave Timing

Figure 5: Serial Peripheral Interface (SPI) Port—Slave Timing

JTAG Test and Emulation Port Timing

Below Table and Figure describe JTAG port operations

JTAG Port Timing

Parameter		Minimum	Maximum	Unit
Timing Parameters				
t_{TCK}	TCK Period	40		ns
t_{STAP}	TDI, TMS Setup Before TCK High	28		ns
t_{HTAP}	TDI, TMS Hold After TCK High	2		ns
t_{SSYS}	System Inputs Setup Before TCK High	28		ns
t_{HSYS}	System Inputs Hold After TCK High	2		ns
				TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		18	ns
t_{DSYS}	System Outputs Delay After TCK Low		18	ns

Note: For TDI/TMS Input Delay (Min/Max) and TDO Output Delay (Min/Max) Please refer above.

Table 15: JTAG Port Timing
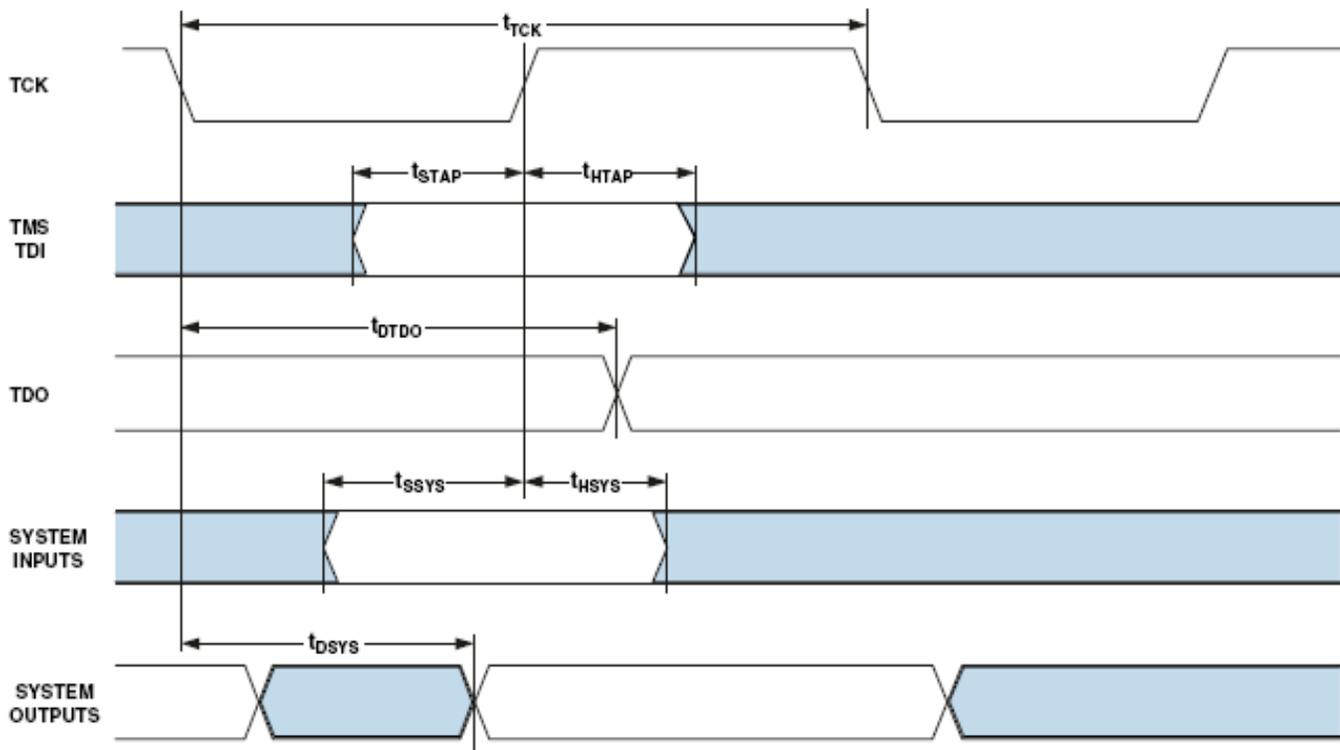
JTAG Port Timing

Figure 6: JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure show typical current-voltage characteristics for the output drivers of the AST-234. The curves represent the current drive capability of the output drivers as a function of output voltage.

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry (PINT) and another due to the switching of external output drivers (PEXT). See the AST-234 Programmers Manual for definitions of the various operating modes and for instructions on how to minimize system power. Many operating conditions can affect power dissipation.

Dynamic Power Units = 1 mW (Internal + Switching)
Leakage Power Units = 1 nW

TEST CONDITIONS

All timing parameters appearing in this datasheet were measured under the conditions described in this section. Figure below shows the measurement point for AC measurements (except output enable/disable). The measurement point VMEAS is TBD V for VDDEXT (nominal) = TBD V.

Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Figure 7: Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output balls are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP} (high) or V_{TRIP} (low). V_{TRIP} (high) is TBD V and V_{TRIP} (low) is TBD V for VDDEXT (nominal) = TBD V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time tENA is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple balls (such as the data bus) are enabled, the measurement value is that of the first ball to start driving.

Output Disable Time Measurement
Output balls are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY}.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load CL and the load current IL.

This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to TBD V for VDDEXT (nominal) = TBD V. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. CL is the total bus capacitance (per data line), and IL is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications.
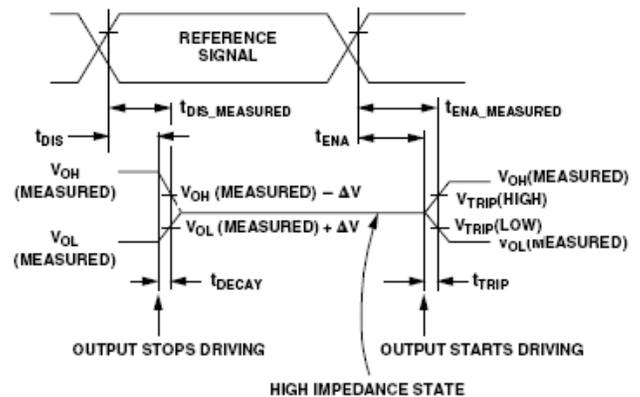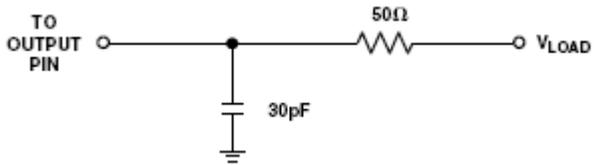
Output Enable/Disable

Figure 8: Output Enable/Disable

Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 9: Equivalent Device Loading for AC Measurements (Includes All Fixtures)

75-BALL VFBGA BALL ASSIGNMENT

Ball No	Signal Name
A1	BOOT_MODE_1
A2	BOOT_MODE_0
A3	GPS_INT
A4	PTTI
A5	GPIO1
A6	GPIO3
A7	GPIO2
A8	GPIO9
A9	GPIO4
B1	SIGN
B2	NC
B3	NC
B5	GPIO0
B6	TDO
B7	TMS
B8	GPIO8
B9	GPIO10
C1	MAGN
C2	NC
C3	NC
C4	GPS_RESET_N
C5	VCC_3V3
C7	TDI
C8	NTRST
C9	GPIO11
D1	CAN_RX
D2	NC
D3	NC
D4	VCC_1V2
D5	VSS
D7	VCC_3V3
D8	TCK
D9	MRESET_N
E1	CAN_TX
E2	NC
E3	VCC_1V2
E4	VSS
E5	VSS
E6	VSS
E7	NC
E9	REF_CLK

Ball No	Signal Name
F1	UART2_TX
F2	NC
F3	TWI_SDA
F4	VSS
F7	SPI_CS
F8	VCC_1V2_BAT
F9	XOUT
G1	UART2_RX
G2	NC
G3	NC
G4	NC
G5	USB_VBUS
G6	NC
G7	NC
G8	VCC_1V2_BAT_IO
G9	XIN
H1	UART1_TX
H2	TWI_SCL
H3	NC
H4	NC
H5	NC
H6	NC
H7	SPI_MISO
H8	SPI_FLASH_CS
H9	VDD_ISO_ENABLE
J1	UART1_RX
J2	USB_DM
J3	USB_DP
J4	SPORT_XFS
J5	SPORT_YADATA
J6	SPORT_XADATA
J7	SPORT_XCLK
J8	SPI_MOSI
J9	SPI_CLK

Table 16: 75-Ball VFBGA Ball Assignment

OUTLINE DIMENSIONS

The Package is 5mm X 5mm. Dimensions in below Figure-30 with 75-Ball VFBGA are shown in millimeters.

SURFACE MOUNT DESIGN
The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard
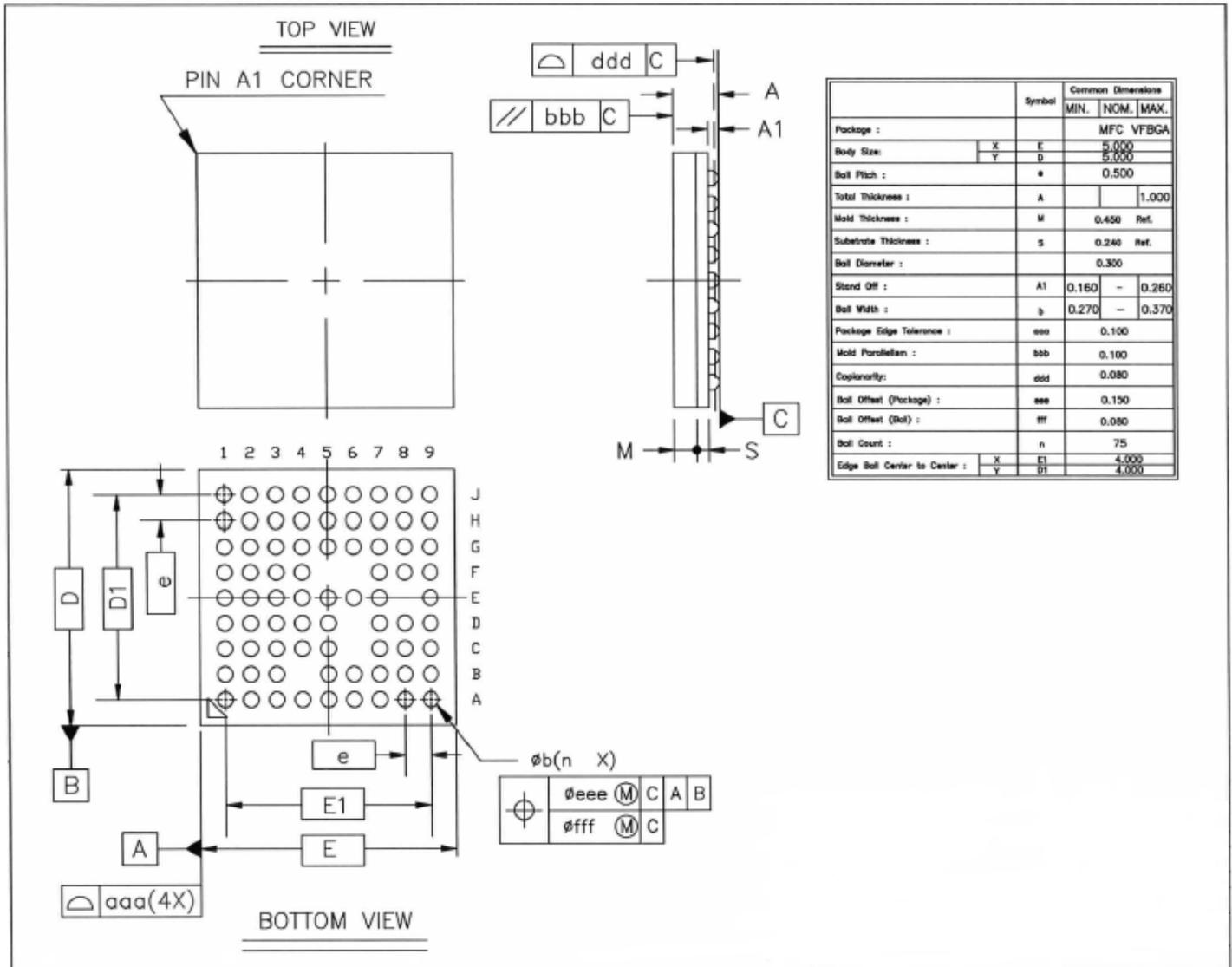

Symbol		MIN.	NOM.	MAX.
			Common Dimensions	
				MFC VFBGA
Package :				MFC VFBGA
Body Size: X	E		5.000	
Y	D		5.000	
Ball Pitch :	e		0.500	
Total Thickness :	A			1.000
Mold Thickness :	M		0.450 Ref.	
Substrate Thickness :	s		0.240 Ref.	
Ball Diameter :			0.300	
Stand Off :	A1	0.160	–	0.260
Ball Width :	b	0.270	–	0.370
Package Edge Tolerance :	eee		0.100	
Mold Parallelism :	bbb		0.100	
Coplanarity:	ddd		0.080	
Ball Offset (Package) :	eee		0.150	
Ball Offset (Ball) :	fff		0.080	
Ball Count :	n		75	
Edge Ball Center to Center : X	E1		4.000	
Y	D1		4.000	

Figure 10: 75 –Ball VFBGA

ORDERING GUIDE

Ordering Guide

Model	Temperature Range	Package Description	Package Option	Operating Voltage
AST-234	-40 ^{0}C to +85 ^{0}C	VFBGA - 0.5 mm pitch (75 balls), 5.0 mm x 5.0 mm x 1.0 mm	75 balls	1.2 V(Internal), 2.5 V / 3.3 V I/O

Table 17. Ordering Guide