Preliminary
Technical Data

AST-GLSRF

GLONASS Downconverter

FEATURES

- Single chip GLONASS downconverter
- GLONASS L1 band (1602 MHz) receiver
- 2.7 V to 3.3 V power supply
- On-chip LNA
- On-chip PLL including complete VCO
- On-chip IF Band Pass Filter
- 50 dB AGC dynamic range
- SIGN and MAGN outputs
- PLL lock information
- Open / Short Antenna control
- Low power operation 15 mA @ 3 Volt
- Supports power-down mode

APPLICATIONS

- Automatic Vehicle Tracking
- Fleet Management
- Security Applications
- Asset Tracking
- Car Telematics / Navigation
- Marine Navigation
- Portable Receivers

GENERAL DESCRIPTION

AST-GLSRF is a high performance, fully integrated, RF front-end chip for downconversion and amplification of GLONASS signals. AST-GLSRF is a superheterodyne receiver designed for LI (1602 MHz), with an on-chip low noise amplifier (LNA), local oscillator, one downconversion IF stage (at 6.120MHz), an automatic gain controlled amplifier (AGC) and on chip IF low pass filter and a 2-bit analog-to-digital converter (ADC).

The ADC either gets sampling clock from internal clock generator (26.598MHz) or through external clock through CKIN pin. The selection is made through CONF1 and CONF2 pins

Some additional features allow to the system to check antenna connection and behavior.

The chip can be interfaced with any active / passive GLONASS antenna.

FUNCTIONAL BLOCK DIAGRAM

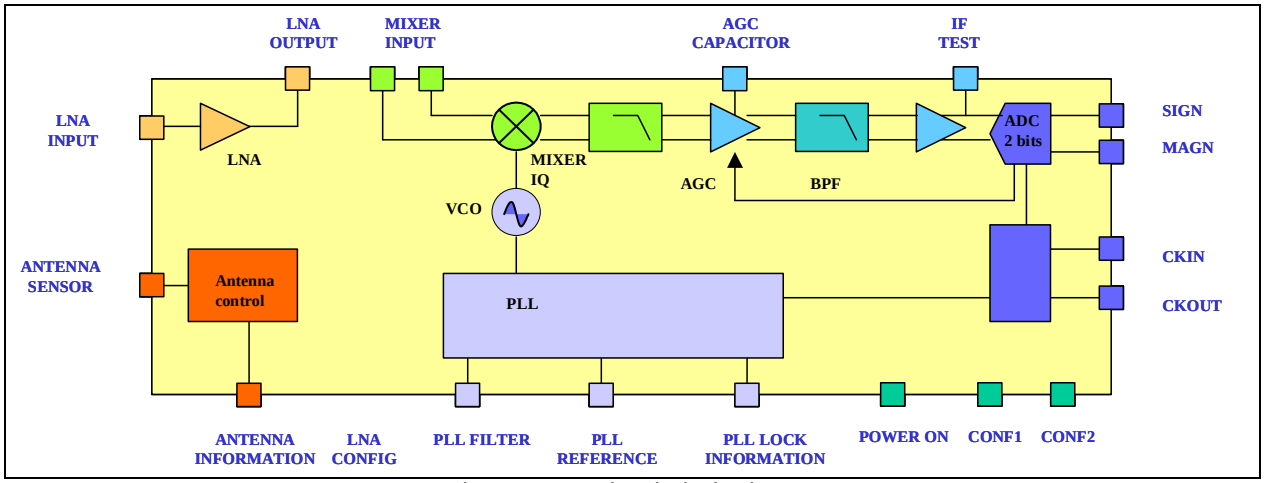

Figure 1. Functional Block Diagram

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REVISION HISTORY
26/08/2011-Revision 1.0

EXPECTED SYSTEM PERFORMANCES

Typical use is: V_{CC} = 2.7 V, and T_A @ 25°C, CONF1 = 1, CONF2 =X, POWERON = 1, IF_TEST pin unconnected.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency		1597.8	1602	1605.6	MHz
Final bandwidth			7.3125		MHz
LO frequency	Through IF frequency measurement		1595.88		MHz
IF frequency			6.120		MHz
Sample frequency			16.368		MHz
Reference			16.368		MHz
Total Power gain	With passive antenna (PA)		80		dB
AGC dynamic range			50		dB
Noise Figure	Typical use (PA)		31		dB
Image frequency reduction		15	20		dBc
Input IP3 (LNA)			-15		dBm
Input IP3 (MIXER)	First stage contribution		-7		dBm
Maximum input power (LNA)	Typical use		-30		dBm
Maximum outband jammer	At LNA input (PA)		-50		dBm
Maximum in-band jammer	At LNA input (PA)		-105		dBm
IF filter bandwidth			7.3125		MHz
Filter rejection @ +/- 8MHz	See note BPF characteristics	15	17		dBc
Voltage		2.7	3.0	3.3	V
Power consumption active	Typical use		16	19	mA
Power Consumption standby	Chip fully powered off			50	uA
Package temperature Range		-40	25	85	C

Table 1. EXPECTED SYSTEM PERFORMANCE

SPECIFICATIONS

Recommended operating conditions: V_{CC} = 2.7 V to 3.3 V, V_{EE} = 0 V, typical is at V_{CC} = 3 V, and T_A @ 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
LNA CHARACTERISTICS (CONF1 = 0 && CONF2 = X)	See the LNA matching network section				
RF frequency		1597.8	1602	1605.6	MHz
Input impedance	Typical simulation		32 – j34		Ω
Input VSWR	With external matching network		1.3	2	
Output impedance	Typical simulation		33 – j112		Ω
Output VSWR	With external matching network		1	2	
S21 (power)	With external matching network	18	20	23	dB
IP1		-30	-26		dBm
IIP3	Typical simulation		-15		dBm
Noise Figure	Typical simulation		2.5		dB
Current consumption (VCC_LNA)	Typical simulation		4.8		mA
LNA CHARACTERISTICS low power (CONF1 = 1 && CONF2 = 0)	See the LNA matching network section				
S21 (power)	With external matching network		13		dB
IP1					dBm
IP3	Typical simulation				dBm
Noise Figure	Typical simulation				dB
Current consumption (VCC_LNA)	Typical simulation				mA
LNA CHARACTERISTICS high power (CONF1 = 1 && CONF2 = 1)	See the LNA matching network section				
S21 (power)	With external matching network		21		
IP1			-22		

IIP3	Typical simulation		-12		
Noise Figure	Typical simulation		1.9	2.5	
Current consumption (VCC_LNA)	Typical simulation		5.7		
MIXER CHARACTERISTICS / AGC	See the Mixer matching network section (100 Ω dual ended)				
RF frequency		1597.8	1602	1605.6	MHz
LO frequency			1595.88		MHz
IF frequency	Typical simulation		6.12		MHz
Input impedance (dual ended)	Typical simulation		150 – j60		Ω
Input VSWR	First mixer stage contribution		1.9	2	
IIP3	Typical simulation	-10	-7		dBm
RF image frequency			1589.76		MHz
S21 Image rejection	Typical simulation	15	20		dBc
DSB noise figure mixer	Typical simulation (VCC_MIX)		15	16	dB
Current consumption Mixer			2		mA
REFERENCE CHARACTERISTICS	See reference clock section				
Input magnitude level (TCXO input)		0.1	0.4	0.5	V p-p
Reference frequency			16.368		MHz
VCO CHARACTERISTICS	See PLL filter section				
Nominal frequency	195 times the reference		3191.76		MHz
Maximum Frequency (VTUNE pin high)		3.2			GHz
Minimum Frequency (VTUNE pin low)			3	3.1	GHz
Phase noise (free running VCO)	@ 100 KHz		-90	-80	dBc / Hz

Phase noise (closed loop)	With a 100 KHz loop bandwidth		-90	-80	dBc / Hz
Spurious (closed loop) @ reference	Typical simulation			-40	dBc
VCO slope	Typical simulation		110		MHz / V
Current pump charge	Typical simulation	+/-75	+/-130	+/-170	µA
Current consumption (VCC_VCO)			1.8		mA
IF CHARACTERISTICS	See AGC / ADC section				
IF frequency	With the reference frequency		6.120		MHz
IF_test regulated level (BPF output selected)	Typical level		-55		dBm
IF_test regulated level (AGC output selection)	Typical level		-60		dBm
S21 (Mixer input -> IF_test)					
Max			35		dB
Max normal	To guarantee the minimum quantization losses		30		dB
Min normal	To guarantee the minimum quantization losses		-20		dB
Min			-35		dB
IP1dB					
for S21 = maximum	Typical simulations		-85		dBm
for S21 = 30 dB	Typical simulations		-70		dBm
for S21 = minimum	Typical simulations		-30		dBm
AGC dynamic range		50	55	65	dB
AGC slope	Typical simulations for a gain within +/–30 dB range		60		dB / V
Magnitude bit duty cycle Used for AGC regulation point	Maintain this rate allow the AST-GLSRF to fix the conversion loss below 0.6 dB.	23	33	43	%
AGC band pass	Typical simulations With a 10 nF load on CAMP pin	1	3	10	KHz

OP1	At ADC input		2.5		dB
LSB	Typical simulations		120		mV
Output test attenuation	BPF output selected		50		dB
Output test attenuation	AGC output selected		35		dB
Output impedance	See AGC / ADC section		250		Ω
Low Pass Filter CHARACTERISTICS					
Center Frequency			6.120		MHz
IF filter bandwidth @ 3dB			7.3125		MHz
IF Filter Ripple			2	3	dB
IF Filter rejection					dB
IF Filter rejection	@ 16 MHz	7	9		dBc
IF Filter rejection	@ 26 MHz	20			dBc
Current consumption (VCC_IF)	Typical simulations				
Gain Max	30 dB gain		4.8		mA
Gain nominal (passive antenna case)	20 dB gain		4.4		mA
Gain (active antenna case)	0 dB gain		4.1		mA
Gain min	-30 dB gain		3.8		mA
ADC / PILOTE / PLL current consumption (VCC_PLL)	Typical simulations CKOUT OFF		4.1		mA
ANALOG LEVELS (typical use)		2.7	3V	3.3	V
LNAIN pin			0.833		V
LNAOUT pin		V_{CC}	V_{CC}	V_{CC}	V
MIXERINP, MIXERINP pins		0.54	0.7	0.85	V
VTUNE pin			0 / V_{CC}		V
REF pin	With 10 KΩ resistor	1.35	1.50	1.65	V

IF_TEST pin			2		V
CAMP pin			0.5 / V_{CC}		V
ANT_SENSE pin	No external connection	0	0	0	V
INPUT CMOS LEVELS					
POWER_ON, CONF1, CONF2, CKIN					V
Input CMOS level V_{IH}		V_{CC}*0.7			V
Input CMOS level V_{IL}				0.3*V_{CC}	V
OUTPUT CMOS LEVELS MAGN, SIGN, PLL_LOCK, ANT_INFO	Typical simulations @ 400 KHz				
Output CMOS level V_{OH}		V_{CC}*0.85			V
Output CMOS level V_{OL}				0.15*V_{CC}	V
Maximum rating output load			5	10	pF
Skew between CKOUT and MAGN / SIGN	See AGC / ADC section Typical simulations with 10 pF load		1	20	ns
Skew between REF and MAGN / SIGN	Typical simulations with 10 pF load		18 ns		ns
Antenna connection information	See Antenna control section				
ANT_SENSE voltage for Antenna connected				V_{CC} – 0.1	V
ANT_SENSE voltage for Antenna disconnected		V_{CC} – 0.05			V
PLL lock information	See PLL LOCK PIN section				
CKOUT clock frequency	Reference frequency * 13 / 8		26.598		MHz
CKIN	Sampling clock input			33	MHz
Total Power consumption					
Power On mode	2.7 Volt / Conf min / Gain 10 dB	13.5			mA

Power On mode	3 Volt / Conf nom / Gain 30 dB	17.5			mA
Standby mode	CKOUT active	1			mA
Standby mode	CKOUT OFF	50			µA

Table 2.SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{CC} to V_{EE}[1]	−0.3 V to +3.6 V
Analog I/O Voltage to V_{EE}	−0.3 V to V_{CC} + 0.3 V
Digital I/O Voltage to V_{EE}	−0.3 V to V_{CC} + 0.3 V
RF maximum power	0 dBm (TBC)
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Maximum Junction Temperature	−40°C to +110°C
Range	

Table 3. ABSOLUTE MAXIMUM RATINGS

[1] V_{EE} = 0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of < 2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

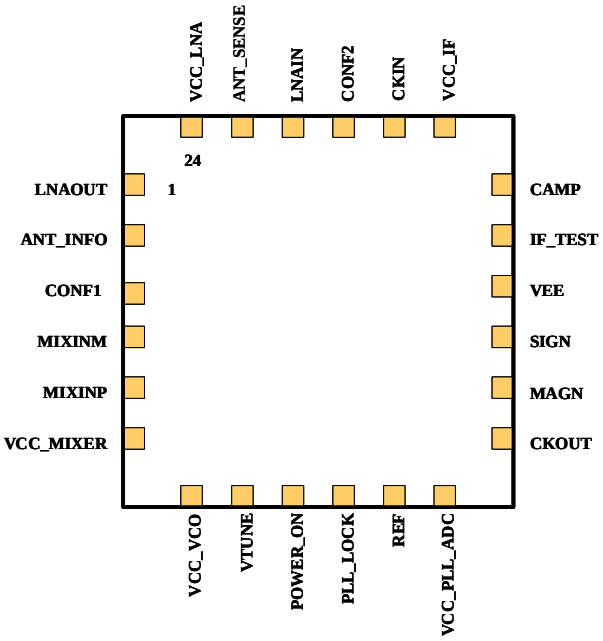

Figure 2. Pin Configuration

Pin Function Descriptions

Pin No.	Mnemonic	Pin Type	Input / Output	Description
1	LNAOUT	Analog	Output	LNA RF Signal, (1597 - 1606 MHz)
2	ANT_INFO	Analog	Output	Antenna connection information pin
3	CONF1	CMOS	Input	Configuration pin
4	MIXINM	Analog	Input	Positive MIXER RF Signal, (1597 – 1606 MHz)
5	MIXINP	Analog	Input	Negative MIXER RF Signal, (1597- 1606 MHz)
6	VCC_MIX	Supply		MIXER Supply
7	VCC_VCO	Supply		VCO Supply
8	VTUNE	Analog		External PLL filter connection
9	POWER_ON	CMOS	Input	Power-On mode pin
10	PLL_LOCK	Analog	Output	PLL LOCK information pin
11	REF	Analog	Input	Reference Clock
12	VCC_PLL_ADC	Supply		PLL / ADC Supply
13	CKOUT	CMOS	Output	Reference frequency
14	MAGN	CMOS	Output	Magnitude Bit Data
15	SIGN	CMOS	Output	Sign Bit Data
16	VEE	Ground		Paddle ground internal connection / redundant with exposed pad (paddle)
17	IF_TEST	Analog	Output	IF test
18	CAMP	Analog		Amplitude bit capacitor signal
19	VCC_IF	Supply		IF Supply
20	CKIN	CMOS	Input	Optional Sampling clock. Selectable with CONF1 and CONF2 combination
21	CONF2	CMOS	Input	Configuration pin
22	LNAIN	Analog	Input	LNA RF Signal, (1597 - 1606 MHz)
23	ANT_SENSE	Analog	Input	Antenna sense for connection control
24	VCC_LNA	Supply		LNA Supply

Table 4. Pin Function Description

THEORY OF OPERATION

POWER SUPPLIES

The AST-GLSRF uses five different power supply groups as follows:

a. VCC_LNA and VEE_LNA
b. VCC_MIX and VEE_ MIX
c. VCC_VCO and VEE_ VCO
d. VCC_IF and VEE_IF
e. VCC_PLL_ADC and VEE_PLL_ADC

These separate power groups increase isolation between internal components. Each power supply group is externally decoupled by a single low value capacitor for oscillation risk reduction.

Decoupling capacitor used for Power supplies

Component Name	Typical value	Unit
C1 C2	100 10	pF nF

Table 5. Decoupling capacitor used for Power supplies

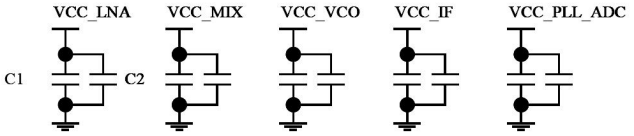

Figure 3. Power supply connections

ISOLATION

Antenna and LNA output
Lna out <->Mixin / VCC_mix <->Vtune / Vtune <->REF / MAG-SIGN <-> LNAIN

MATCHING NETWORK

The RF input has unmatched input impedance. The necessary 50 Ω RF external input-matching components must be mounted as close to the RF input as possible. Input and output matching networks provide 50 Ω source and load impedance.

LNA MATCHING NETWORK

LNA input is internally biased; therefore, it should be externally ac-coupled.

Tests were made with lumped matching elements, performing maximum power transfer between LNA and input and output. Input matching impedances given in Table 6 are designed for simultaneous input and output matching.

Input and output RF signals should be connected to the external devices via a 50 Ω line.

External components used for LNA matching

Component Name	Typical value	Unit
C1 C2 C3 L1 L2 L3	NC 100 1.8 4.2 2.2 2.2	pF pF pF nH nH nH

Table 6. External components used for LNA matching

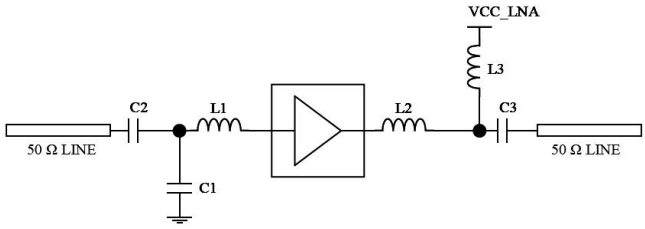

Figure 4. LNA matching network connections

MIXER MATCHING NETWORK

The mixer structure is double-balanced. The local oscillator (LO) input and IF output are fully differential. The RF differential port inputs has a 100 Ω matched impedance and is internally biased, so it must be externally ac-coupled.

External components used for Mixer matching

Component Name	Typical value	Unit
C1* C2*	100 100	pF pF

Table 7. External components used for Mixer matching

***** *Not required if a SAW filter is used or BPF with internal ac-coupling.*

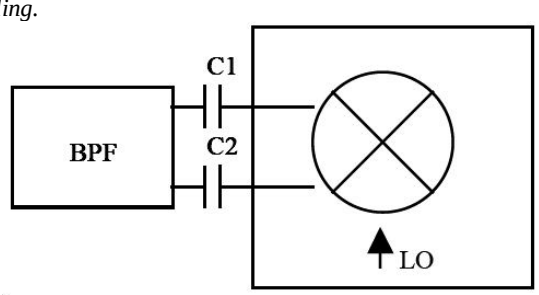

Figure 5. Mixer matching network connection

It is possible to connect a single ended 50Ω Band pass filter to the mixer by connecting the BPF to either

MIXINM / MIXINP and the other mixer input pin to ground using 100pF capacitor.

REFERENCE CLOCK GENERATION

The clock input pin REF is internally biased and must be externally ac-coupled. The PLL works on the rising edge of the TCXO.

External components used for reference input

Component Name	Typical value	Unit
C1	10	nF

Table 8. External components used for reference input

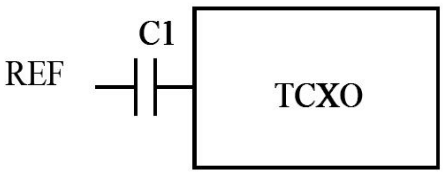

Figure 6. Reference clock connections

PLL FILTER

The PLL generates the local oscillation. It includes a VCO with an on-chip tank circuit, dividers, and a phase detector with external loop filter components. A reference frequency is required for the PLL. The PLL is a second- or a third-order loop, Type 2 for zero frequency error.

The VCO is a monolithic LC voltage controlled oscillator.
The divider divides the local oscillator (LO) frequency by 195 before comparing with the reference frequency (REF).

The design of the PLL depends on two criteria: the filtering of the reference frequency signal and the phase noise of the output signal of the PLL. The phase noise of the VCO is filtered by the PLL.
The PLL includes a charge-pump active filter to perform second-order loop. The PLL loop filter components are selected to give a PLL loop bandwidth of approximately 50 / 100 KHz to minimize phase noise.
An additional on-chip LPF (R = 10 kΩ and C = 10 pF) is present in series in the VTUNE command and allows better rejection harmonics of the comparison frequency.

Figure 7 shows the PLL filter configuration and Table 9 lists the values.

External components used for the PLL filter

Component Name	Typical value	Unit
C1 C2 R2	2.7 100 3.3	nF pF KΩ

Table 9. External components used for the PLL filter

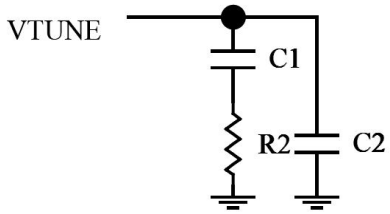

Figure 7. PLL filter connections

AGC / ADC

The internal band pass filter provides the necessary filtering for the system requirement. An auto-calibration is set during the PLL lock phase at each power on and allows centering the filter for the application.

The IFTEST output is used for test purposes only to check the whole RF / IF chain gain. IFTEST pin will output AGC output or ADC input based on ANTENNA_SENSE pin configurations. Refer Antenna Control Pins configuration for more information.

The output impedance of IF TEST pin is around 250 Ω.

External components used for IF TEST

Component Name	Typical value	Unit
C1	10	nF
R1	10	KΩ

Table 10. External components used for IF TEST

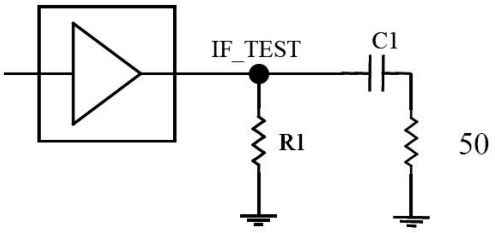

Figure 8.Equivalent IF CHAIN

The power on IFTEST output is measured on a 50 Ω load connected on IFTEST (ac coupled). To get the whole RF /

IF gain from the mixer input up to the ADC input or BPF input the following attenuation should be added:

Attenuation on IFTEST

AGC / BPF	Formula	Unit
Att AGC	19+20LOG[50/(250+50)]=35	dB
Att BPF	34+20LOG[50/(250+50)]=50	dB

Table 11. Attenuation on IFTEST

To maximize the signal-to-noise ratio (SNR) with a 2-bit ADC, the AGC regulation point is fixed at 1σ to activate the amplitude bit 33% of the time. This mean time allows the AST-GLSRF to fix the conversion loss below 0.6 dB.

The rms swing at the ADC input is maintained roughly at 120mV providing a –55 dBm level at the IFTEST output. In this technical data document the gain information is provided with the attenuation displayed in the table above.

The CAMP pin can be biased from outside to control the AGC gain.

Table 12 shows the relation between IF2 the signal at the ADC input and the LSB the magnitude reference level. The data rate of the ADC is dependent on the sampling clock.

SIGN and MAGN logic level versus IF2 magnitude level

IF2 Magnitude level	SIGN Logic level	MAGIN Logic level
LSB < IF2 0<IF2 < LSB -LSB < IF2 < 0 IF2 < -LSB	1 1 0 0	1 0 0 1

Table 12. SIGN and MAGN logic level versus IF2 magnitude level

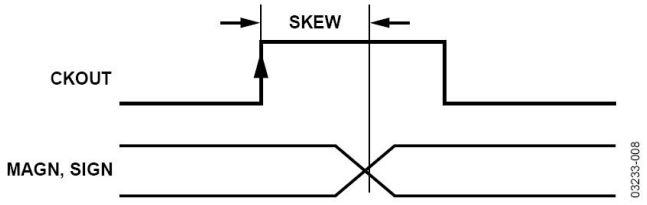

Figure 9. CKOUT to MAGN / SIGN Skew

A capacitor is to be used at CAMP pin to reduce the effect of a strong spurious noise on AGC filter as well as to stabilize of AGC.

External components used with the AGC

Component Name	Typical value	Unit
CAMP	20	NF

Table 13. External components used with the AGC

ADC sampling clock selection

ADC sampling clock can be either internal (26.598MHz CKPLL) or through CKIN pin. The selection for this is done through CONF1 and CONF2 pins. In case CKIN is not used, it can be grounded

For sampling clock selection refer to chapter CONF1 AND CONF2 PINS

POWER ON / STANDBY MODE PIN

One digital input pin POWER_ON permits the AST-GLSRF circuit to enter standby mode. During standby mode all blocks are turned off except CKOUT based on configuration pins.

POWER ON Logic Control Signal

MODE	Logic Level POWER ON
Active Stand By	0 1

Table 14. POWER ON Logic Control Signal

PLL LOCK PIN

One digital output pin PLL_LOCK permits the AST-GLSRF circuit to provide information on PLL behavior.

PLL_LOCK Logic Control Signal

INFORMATION	Logic Level PLL_LOCK
PLL unlocked PLL locked	0 1

Table 15. PLL_LOCK Logic Control Signal

An external capacitor is required for PLL lock pin.

External components used for the pll lock

Component Name	Typical value	Unit
C	10	nF

Table 16. External components used for the pll lock

BPF

When PLL_LOCK kept at zero bias voltage, the self-tuning of BPF is disabled. This way BPF characteristics depend on process, temperature or power supply state.

CONF1 AND CONF2 PINS

These two pins permit AST-GLSRF to increase or decrease chip performance with regard to power save mode or better jammer robustness.
The table below specifies nominal use, low power use and high jammer robustness.

Configuration Logic Control Signal / Power on

Mode: Power On active (1)	Logic Level CONF1	Logic Level CONF2
CKIN selected / ckout buffer OFF	0	0
CKPLL selected / ckout clock OFF	0	1
CKIN selected / ckout buffer OFF	1	0
CKPLL selected / ckout clock OFF	1	1

Table 17. Configuration Logic Control Signal / power on

Configuration Logic Control Signal / Power off

MODE: Power ON standby (0)	Logic Level CONF1	Logic Level CONF2
Chip not fully power down	0	0
Chip not fully power down: CKOUT = CKIN	0	1
Chip not fully power down	1	0
Chip not fully power down	1	1

Table 18. Configuration Logic Control Signal / power off

ANTENNA CONTROL PINS

One analog input ANT_SENSE and one digital output ANT_INFO pins permit the AST-GLSRF circuit to check the connection of an active antenna. A drop of 100 mV is necessary to get information of antenna connected.
R1 should be set to take in account this internal threshold and the active antenna current consumption. The drop is based on the voltage difference between VCC_LNA and the ANT_SENSE pin.

External components used for the antenna sense

Component Name	Typical value	Unit
L1 R1	33 TBD	nH Ω

Table 19. External components used for the antenna sense

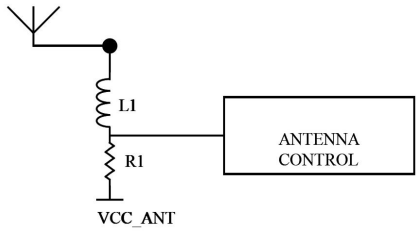

Figure 10.Antenna sensor connections

ANT_INFO Logic Output Signal

INFORMATION	Logic Level ANT_INFO
Antenna disconnected Antenna connected	0 1

Table 20. ANT_INFO Logic Output Signal

ANT_SENSE pin can be used during the test to select the AGC output of the IF chain instead of ADC input.

PLL_LOCK Logic Control Signal

ANT_SENSE pin Voltage	IF_test output selection
$> V_{CC}/2$ $< V_{CC}/2$	ADC input AGC output

Table 21. PLL_LOCK Logic Control Signal

DETAILED BLOCK DIAGRAM

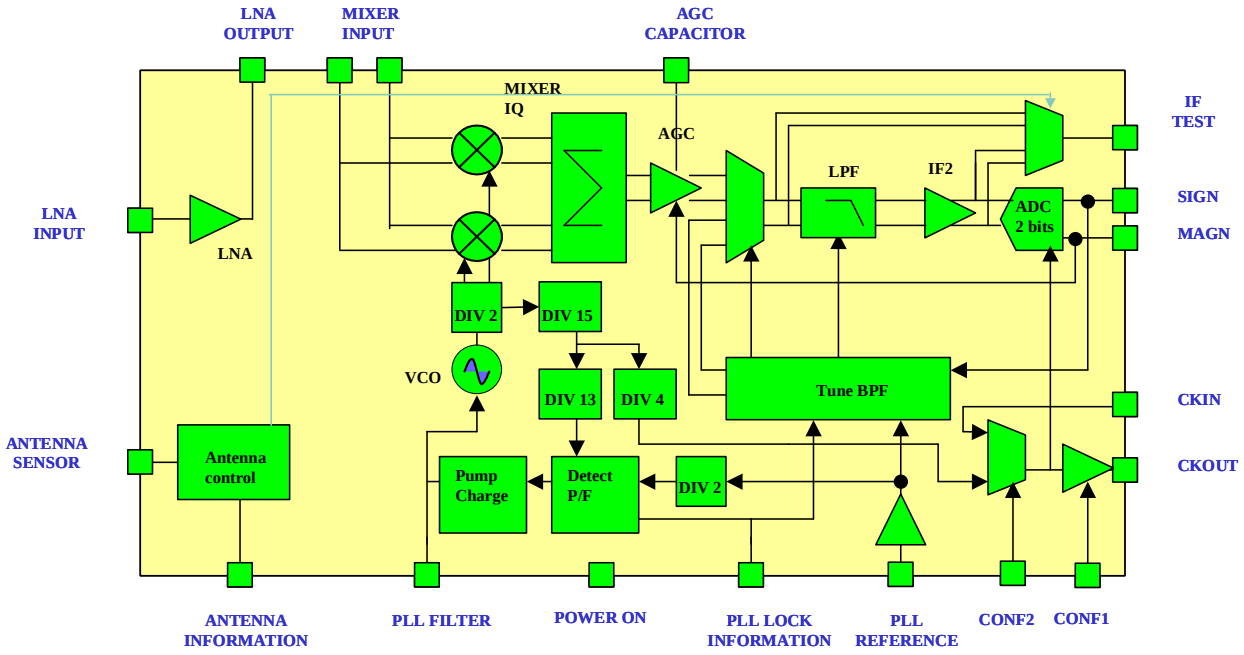

Figure 11. Detailed Block Diagram

CHIP INFORMATION

OUTLINE DIMENSIONS

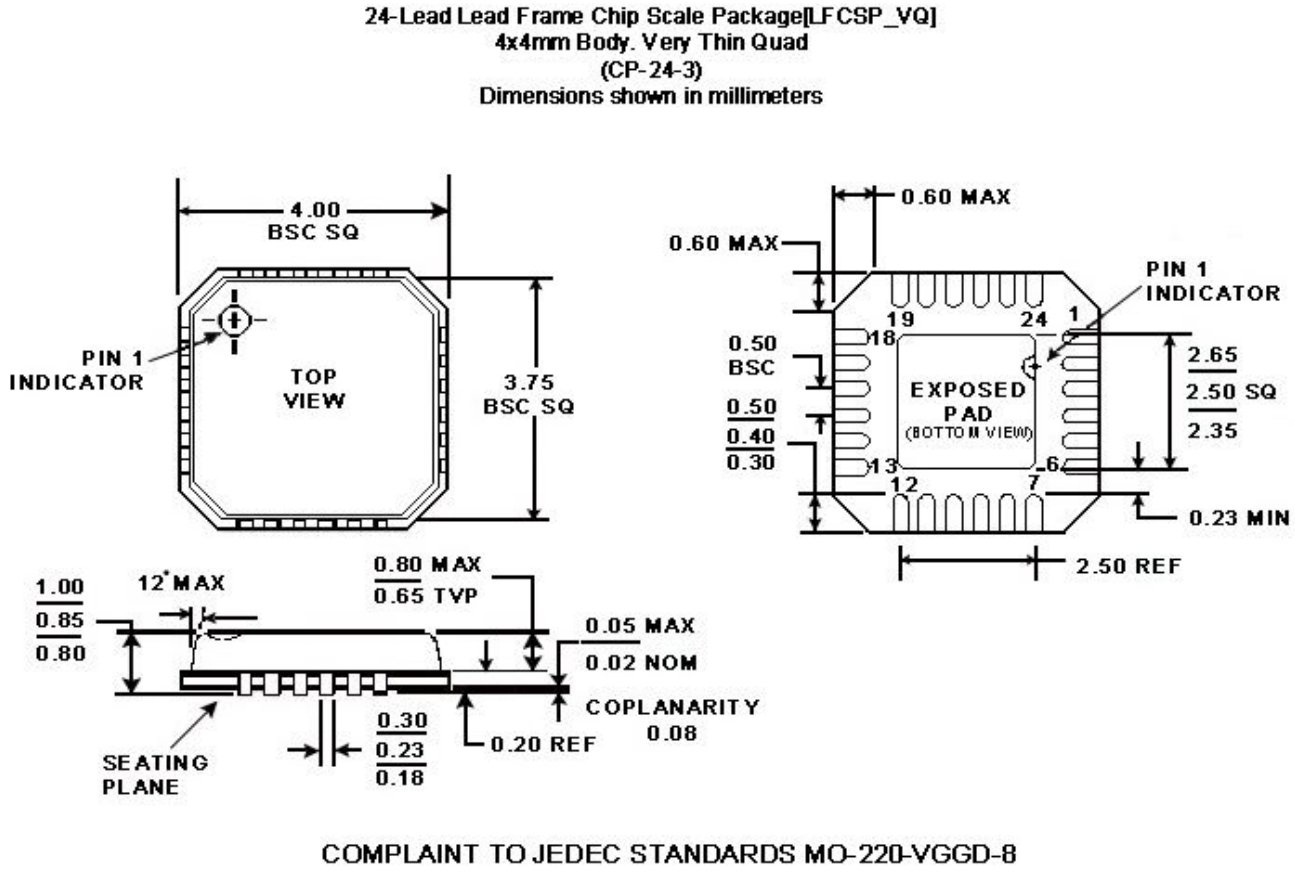

Figure 12. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ] dimensions shown in millimeters

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
AST-GLSRF	3.0 V	−40°C to +85°C	24L LFCSP 4mm x 4mm x 0.85mm Lead Free Package	

Table 22.Ordering Guide

APPLICATION SCHEMATIC

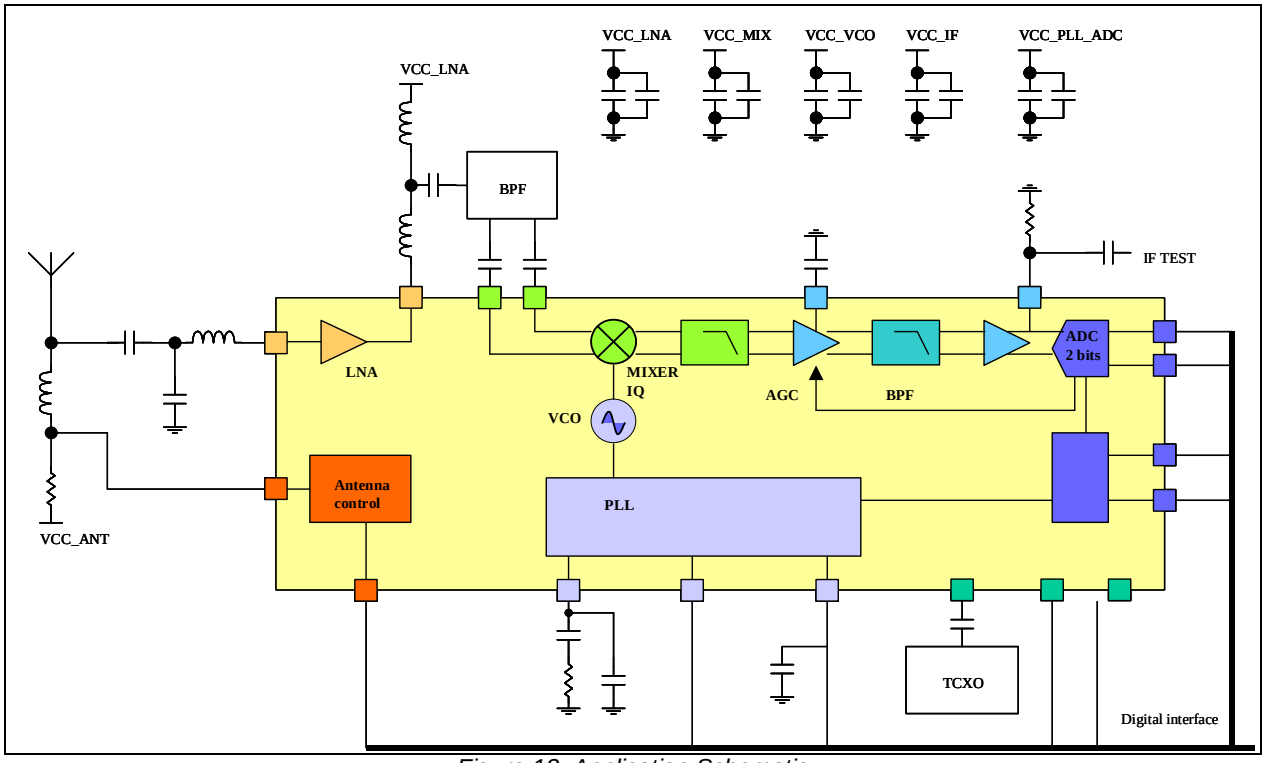

Figure 13. Application Schematic