NAVIKA

AST-GPSRF

GPS / Galileo RF Downconverter

Document History

Sl No.	Version	Changed By	Changed On	Change Description
1	0.1	Sudhir N S	17-Nov-2014	Created

Contents

Features

- Single chip GPS / Galileo downconverter
- GPS L1 band C/A code (1575.42 MHz) receiver
- GALILEO L1 band OS code (1575.42 MHz) receiver
- 2.7 V to 3.3 V power supply
- On-chip LNA
- On-chip PLL including complete VCO
- On-chip IF Band Pass Filter
- 50 dB AGC dynamic range
- SIGN and MAGN outputs
- PLL lock information
- Open / Short Antenna control
- Low power operation 15 mA @ 3.0 Volt
- Supports power-down mode

Applications

- Automatic Vehicle Tracking
- Fleet Management
- Security Applications
- Asset Tracking
- Car Telematics / Navigation
- Marine Navigation
- Portable Receivers

Introduction

AST-GPSRF is a high performance, fully integrated, RF front-end chip for down conversion and amplification of GPS and Galileo signals. It has been designed for L1 (1575.42 MHz), C/A GPS band receivers and OS Galileo band receivers.

AST-GPSRF is a superheterodyne receiver, with an on-chip low noise amplifier (LNA), local oscillator, one downconversion IF stage (at 4.092 MHz), an automatic gain controlled amplifier (AGC), an on chip IF band pass filter and a 2-bit analog-to-digital converter (ADC).

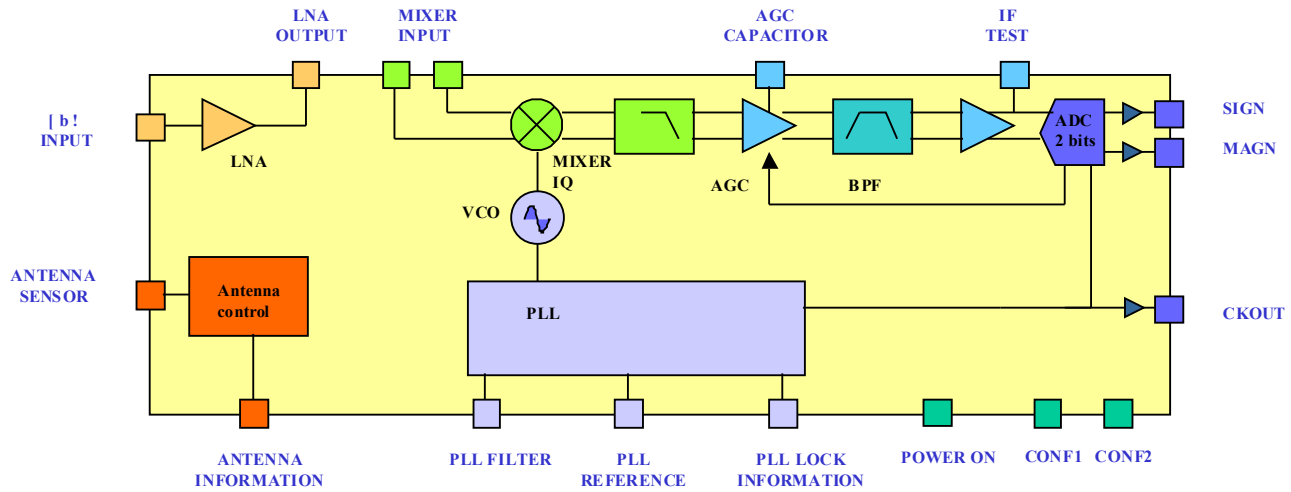
The downconverter works with 16.368 MHz reference clock and sampling clock of 16.368 MHz is internally generated.

The downconverter has internal band pass filter, which does not require external calibration.

Antenna connection and open circuit can be sensed and the information is made available.

The chip can be interfaced with any active / passive GPS antenna.

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

Recommended operating conditions: VCC = 2.7 V to 3.3 V, VEE = 0 V, typical is at VCC = 2.7 V, and TA @ 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency		1573	1575.42	1577	MHz
Input Impedance	With matching network		50		Ω
Input VSWR	With matching network		1.3	2	
Output impedance	With matching network		50		Ω
Output VSWR	With matching network		1	2	
LNA Normal power operation (CONF1 = 0 && CONF2 = X)					
S21 (Power)	With external matching network	18	21	23	dB
IP1		-30	-26		dBm
IIP3	Simulation		-15		dBm
Noise figure	Simulation		1.5	2	dB
LNA Low power operation (CONF1 = 1 && CONF2 = 0)					
S21 (Power)	With external matching network		13		dB
IP1			-27		dBm
IIP3	Simulation		-17		dBm
Noise figure	Simulation		1.8	2.2	dB
LNA High power operation (CONF1 = 1 && CONF2 = 1)					"
S21 (Power)	With external matching network		19		dB
IP1			-23		dBm
IIP3	Simulation		-12		dBm
Noise figure	Simulation		1.2	2	dB
Mixer characteristics	Refer Mixer matching network section (100Ω dual ended)				
RF frequency		1573	1575.42	1577	MHz
LO frequency			1571.328		MHz
IF frequency			4.092		MHz
Input impedance	Simulation dual ended		150-j60		Ω
Input VSWR	Simulation for 100Ω		1.9	2	
Input impedance	Single ended		50		Ω
Input VSWR	Single ended for 50Ω			2	

Parameter	Conditions	Min	Typ	Max	Unit
IIP3	Simulation	-10	-7		dBm
RF image frequency			1567.23		MHz
S21 Rejection			15		dBc
DSB noise figure			15	16	dB
Reference clock characteristics	**Refer to Reference clock section**				
Input magnitude level (TCXO input)		0.1	0.4	0.5	V p-p
Reference frequency			16.368		MHz
Input load	Simulation		0.5pF parallel with 25KΩ	1pF parallel with 12KΩ	
VCO Characteristics	**Refer PLL filter section**				
Nominal frequency	192 times the reference		3142		MHz
Maximum frequency (VTUNE pin high)	Simulation	3300			MHz
Minimum frequency (VTUNE pin low)				3100	MHz
Phase noise (free running VCO)	@100KHz (Simulation)		-90	-80	dBc / Hz
Phase noise (closed loop)	With 100kHz loop bandwidth (Simulation)		-90	-80	dBc / Hz
Spurious (Closed loop) @ reference	Simulation			-40	dBc
VCO slope	Simulation		0.160		GHz / V
Current pump charge	Simulation	+/-50	+/-90	+/-150	µA
IF Characteristics	**Refer AGC / ADC section**				
IF frequency	With reference frequency		4.092		MHz
Level at IF_test pin	With R and C network with 50Ω measuring equipment		-55	3100	dBm
Maximum gain (S21 from mixer input to ADC input)	With AGC active when the AGC amplifier gain is maximum		62		dB
Minimum gain (S21 from mixer input to ADC input)	With AGC active when AGC amplifier gain is minimum		7		dB
Noise figure for S21 of 50dB	Simulation			15	dB
IP1 for S21 maximum	Simulation		62	-85	dBm

Parameter	Conditions	Min	Typ	Max	Unit
IP1 for S21 = 30dB	Simulation with Vcamp = 1.6V			-70	dBm
IP1 for S21 = minimum	Simulation			-30	dBm
AGC section					
AGC dynamic range		50	55	65	dB
AGC slope			60		dB / V
Magnitude bit duty cycle		23	33	43	%
AGC band pass upper frequency	With 10nF load on CAMP pin	1	3	10	KHz
OP1dB	Simulation		2.5	-70	LSB
IF test point	**With RC network as per AGC / ADC section**				
Output signal attenuation			34		dB
Output impedance			250		Ω
Band Pass Filter CHARACTERISTICS					
Center Frequency			4.092		MHz
IF filter bandwidth @ 3dB			4.092		MHz
IF Filter Ripple	Simulation		2	3	dB
IF Filter rejection	@ 7 MHz	6			dBc
IF Filter rejection	@ 8 MHz	15	17		dBc
IF Filter rejection	@ 14 MHz		20		dBc
DC levels at Analog pins for various V_{CC}		2.7	3.0	3.3	V
LNAIN pin			0.833		V
LNAOUT pin		V_{CC}	V_{CC}	V_{CC}	V
MIXERINP, MIXERINP pins		0.54	0.7	0.85	V
VTUNE pin			0 / V_{CC}		V
REF pin		1.35	1.50	1.65	V
IF_TEST pin	With 10 KΩ resistor		2		V
CAMP pin	With RC network as per AGC / ADC section		0.5 / V_{CC}		V
ANT_SENSE pin	No external connection	0	0	0	V
IBIASBPF pin			0.072		V

Parameter	Conditions	Min	Typ	Max	Unit
Input CMOS signals (POWER_ON, CONF1, CONF2 pins)					
VIH		V_{CC}*0.7			V
VIL				0.3*V_{CC}	V
Output CMOS signals (SIGN, MAGN, PLL_LOCK, ANT_INFO)					
VOH		V_{CC}*0.85			
VOL				0.15*V_{CC}	
Output drive capacity	Refer AGC / ADC section		5	10	pF
Skew between CKOUT and SIGN / MAGN	Simulation with 10pF load		1	20	nsec
Skew between REF and SIGN / MAG	Simulations with 10pF load		18		nsec
Antenna Connection information	**Refer Antenna control section**				
ANT_SENSE voltage to detect Antenna connected				V_{CC} – 0.1	V
ANT_SENSE voltage to detect Antenna disconnection		V_{CC} – 0.5			V
Current consumption of individual sections					
VCC_LNA with LNA at normal gain			4		mA
VCC_LNA with LNA at low gain			2		
VCC_LNA with LNA at high gain			6		
VCC_MIX			2		
VCC_VCO	At AGC gain of 30dB, 25dB and –25dB	3.2	1.5		
VCC_IF			2.9	2.5	
VCC_PLL_ADC			2.2mA		

Parameter	Conditions	Min	Typ	Max	Unit
Total Power consumption					
Power On mode	2.7 Volt / Conf min / Gain 10 dB		12.5		mA
Power On mode	3 Volt / Conf nom / Gain 30 dB		16.3		mA
Standby mode	CKOUT active			1	mA
Standby mode	CKOUT OFF			50	µA

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{CC} to V_{EE}[1]	- 0.3 V to +3.6 V
Analog I/O Voltage to V_{EE}	- 0.3 V to VCC + 0.3 V
Digital I/O Voltage to V_{EE}	- 0.3 V to VCC + 0.3 V
RF maximum power	0 dBm (TBC)
Operating Temperature Range	- 40°C to +85°C
Storage Temperature Range	- 40°C to +150°C
Maximum Junction Temperature Range	- 40°C to +110°C

[1] V_{EE} = 0 V

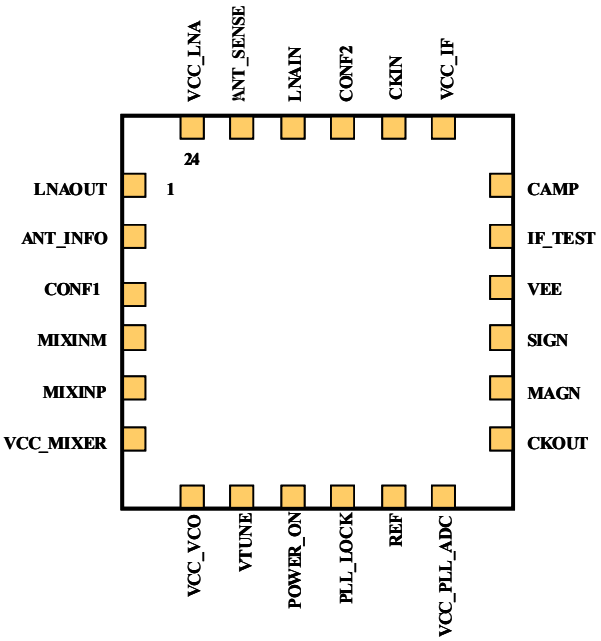
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Pin Function Descriptions

Pin No.	Mnemonic	Pin Type	Input / Output	Description
1	LNAOUT	Analog	Output	LNA RF Signal, (1575.42 MHz)
2	ANT_INFO	Analog	Output	Antenna connection information pin
3	CONF1	CMOS	Input	Configuration pin
4	MIXINM	Analog	Input	Positive MIXER RF Signal, (1575.42 MHz)
5	MIXINP	Analog	Input	Negative MIXER RF Signal, (1575.42 MHz)
6	VCC_MIX	Supply		MIXER Supply
7	VCC_VCO	Supply		VCO Supply
8	VTUNE	Analog		External PLL filter connection
9	POWER_ON	CMOS	Input	Power-On mode pin
10	PLL_LOCK	Analog	Output	PLL LOCK information pin
11	REF	Analog	Input	Reference Clock
12	VCC_PLL_ADC	Supply		PLL / ADC Supply
13	CKOUT	CMOS	Output	Reference frequency
14	MAGN	CMOS	Output	Magnitude Bit Data
15	SIGN	CMOS	Output	Sign Bit Data
16	V_{EE}	Ground		Paddle ground internal connection / redundant with exposed pad (paddle)
17	IF_TEST	Analog	Output	IF test
18	CAMP	Analog		Amplitude bit capacitor signal
19	VCC_IF	Supply		IF Supply
20	IBIASBPF	Analog		Internal current source for the BPF
21	CONF2	CMOS	Input	Configuration pin
22	LNAIN	Analog	Input	LNA RF Signal, (1575.42 MHz)
23	ANT_SENSE	Analog	Input	Antenna sense for connection control
24	VCC_LNA	Supply		LNA Supply

THEORY OF OPERATION

Power Supplies

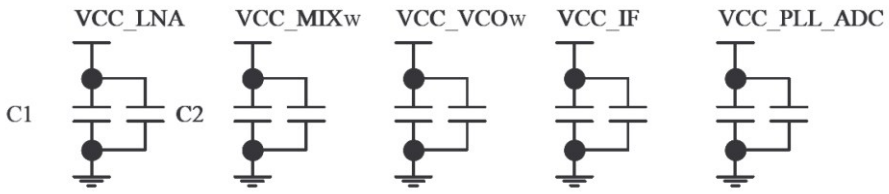
The AST-GPSRF uses five different power supply groups as follows:

- VCC_LNA and VEE_LNA
- VCC_MIX and VEE_ MIX
- VCC_VCO and VEE_ VCO
- VCC_IF and VEE_IF
- VCC_PLL_ADC and VEE_PLL_ADC

These separate power groups increase isolation between internal components. Each power supply group is externally decoupled by a single low value capacitor for oscillation risk reduction.

Decoupling capacitor used for Power supplies

Component Name	Typical value	Unit
C1 C2	100 10	pF nF



Power supply connections

Isolation

Antenna and LNA output

Lna out <->Mixin / VCC_mix <->Vtune / Vtune <->REF / MAG-SIGN <-> LNAIN

Matching Network

The RF input has unmatched input impedance. The necessary 50Ω RF external input-matching components must be mounted as close to the RF input as possible. Input and output matching networks provide 50Ω source and load impedance.

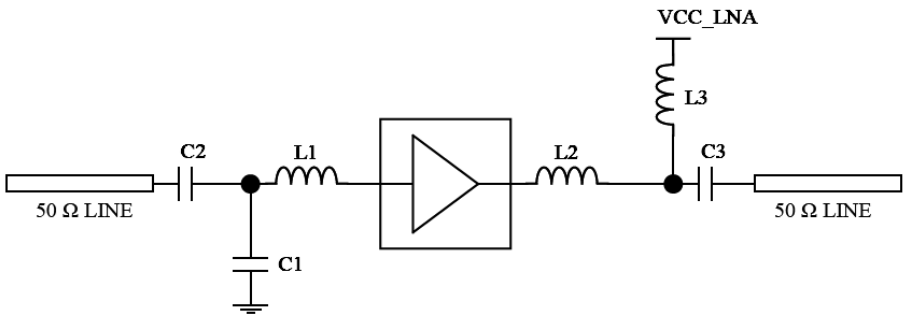
LNA Matching Network

LNA input is internally biased; therefore, it should be externally ac-coupled.

Tests were made with lumped matching elements, performing maximum power transfer between LNA and input and output. Input matching impedances given in Table 6 are designed for simultaneous input and output matching. Input and output RF signals should be connected to the external devices via a 50Ω line.

External components used for LNA matching

Component Name	Typical value	Unit
C1	NC	pF
C2	100	pF
C3	1.8	pF
L1	4.2	nH
L2	2.2	nH
L3	2.2	nH



LNA matching network connections

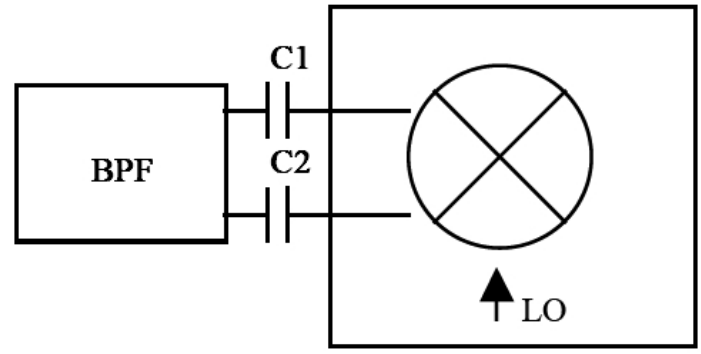
Mixer Matching Network

The mixer structure is double-balanced. The local oscillator (LO) input and IF output are fully differential. The RF differential port inputs has a 100Ω matched impedance and is internally biased, so it must be externally ac-coupled.

External components used for Mixer matching

Component Name	Typical value	Unit
C1* C2*	100 100	pF pF

** Not required if a SAW filter is used or BPF with internal ac-coupling.*



Mixer matching network connection

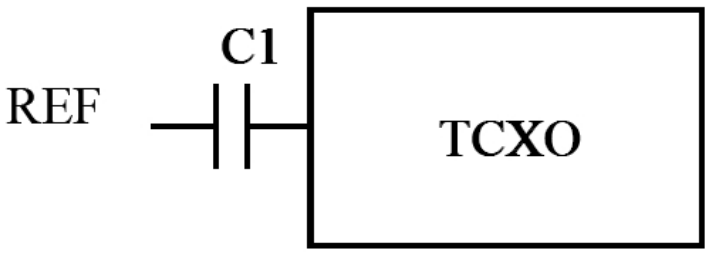
It is possible to connect a single ended 50Ω Band pass filter to the mixer by connecting the BPF to either MIXINM / MIXINP and the other mixer input pin to ground using 100pF capacitor.

REFERENCE CLOCK GENERATION

The clock input pin REF is internally biased and must be externally ac-coupled. The PLL works on the rising edge of the TCXO.

External components used for reference input

Component Name	Typical value	Unit
C1	10	nF



Reference clock connections

PLL FILTER

The PLL generates the local oscillation. It includes a VCO with an on-chip tank circuit, dividers, and a phase detector with external loop filter components. A reference frequency is required for the PLL. The PLL is a second- or a third-order loop, Type 2 for zero frequency error.

The VCO is a monolithic LC voltage controlled oscillator.
The divider divides the local oscillator (LO) frequency by 192 before comparing with the reference frequency (REF).

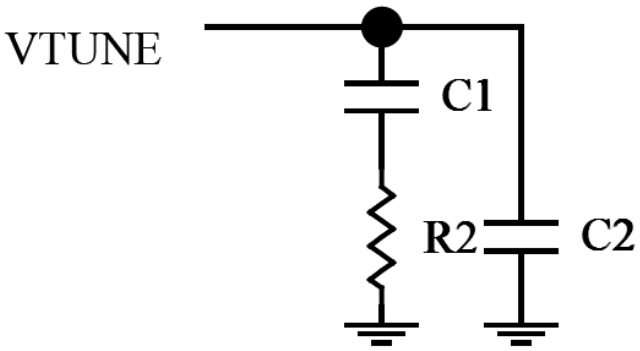
The design of the PLL depends on two criteria: the filtering of the reference frequency signal and the phase noise of the output signal of the PLL. The phase noise of the VCO is filtered by the PLL.

The PLL includes a charge-pump active filter to perform second-order loop. The PLL loop filter components are selected to give a PLL loop bandwidth of approximately 50 / 100 kHz to minimize phase noise.

An additional on-chip LPF (R = 10 KΩ and C = 10 pF) is present in series in the VTUNE command and allows better rejection harmonics of the comparison frequency.

External components used for the PLL filter

Component Name	Typical value	Unit
C1 C2 R2	2.7 100 3.3	nF pF KΩ



Reference clock connections

AGC / ADC

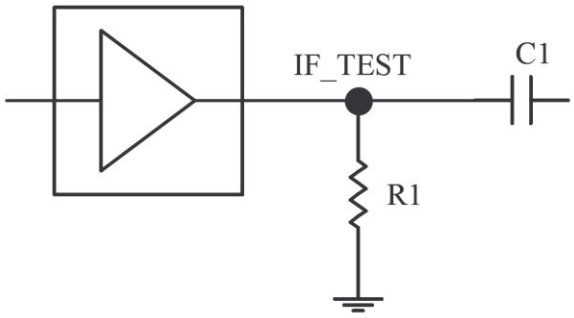
The internal band pass filter provides the necessary filtering for the system requirement. An auto-calibration is set during the PLL lock phase at each power on and allows to center the filter for the application.

The IFTEST output is used for test purposes only to check the whole RF / IF chain gain. IFTEST pin will output AGC output or ADC input based on ANTENNA_SENSE pin configurations. Refer Antenna Control Pins configuration for more information.

The output impedance of IF TEST pin is around 250Ω.

External components used for IF TEST

Component Name	Typical value	Unit
C1 R1	10 10	nF KΩ



Equivalent IF CHAIN

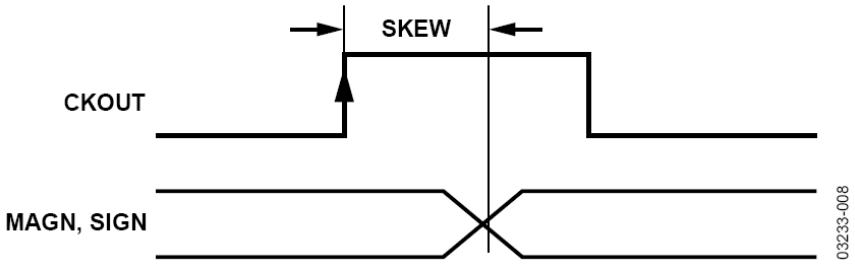
To maximize the signal-to-noise ratio (SNR) with a 2-bit ADC, the AGC regulation point is fixed at 1σ to activate the amplitude bit 33% of the time. This mean time allows the AST-GPSRF to fix the conversion loss below 0.6 dB.

The CAMP pin can be biased from outside to control the AGC gain.

Table 11 lists the levels of SIGN and MAGN bits with respect to the IF2 magnitude. The data rate of the ADC is dependent on the sampling clock employed in the design.

SIGN and MAGN logic level versus IF2 magnitude level

IF2 Magnitude level	SIGN Logic level	MAGIN Logic level
LSB < IF2 0<IF2 < LSB -LSB < IF2 < 0 IF2 < -LSB	1 1 0 0	1 0 0 1



CKOUT to MAGN / SIGN Skew

It is necessary to stabilize the AGC and to set the AGC band-pass to be less sensitive to external strong spurious noise, a capacitor is used on CAMP pin.

External components used with the AGC

Component Name	Typical value	Unit
CAMP	20	nF

POWER ON / STANDBY MODE PIN

One digital input pin POWER_ON permits the AST-GLSRF circuit to enter standby mode. During standby mode all blocks are turned off except CKOUT based on configuration pins.

POWER ON Logic Control Signal

MODE	Logic Level POWER ON
Active Stand By	0 1

PLL LOCK PIN

One digital output pin PLL_LOCK permits the AST-GLSRF circuit to provide information on PLL behavior.

PLL_LOCK Logic Control Signal

INFORMATION	Logic Level PLL_LOCK
PLL unlocked PLL locked	0 1

When kept at zero bias voltage, the self-tuning of BPF is disabled. This way BPF is at the nominal simulation case. The IBIASBPF pin can be used to tune the BPF.

An external capacitor is required for PLL lock pin.

External Components used for the PLL Lock

Component Name	Typical value	Unit
C	10	nF

CONF1 AND CONF2 PINS

These two pins permit AST-GLSRF to increase or decrease chip performance with regard to power save mode or better jammer robustness.

The table below specifies nominal use, low power use and high jammer robustness.

Configuration Logic Control Signal / Power on

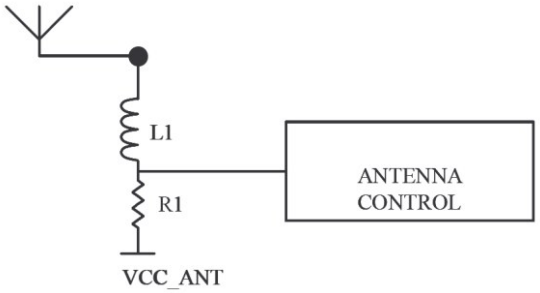
Mode : Power On active (1)	Logic Level CONF1	Logic Level CONF2
CKIN selected / ckout buffer OFF	0	0
CKPLL selected / ckout clock OFF	0	1
CKIN selected / ckout buffer OFF	1	0
CKPLL selected / ckout clock OFF	1	1

Configuration Logic Control Signal / Power off

MODE: Power ON standby (0)	Logic Level CONF1	Logic Level CONF2
Chip not fully power down	0	0
Chip not fully power down: CKOUT = CKIN	0	1
Chip not fully power down	1	0
Chip not fully power down	1	1

ANTENNA CONTROL PINS

One analog input ANT_SENSE and one digital output ANT_INFO pins permit the AST-GPSRF circuit to check the connection of an active antenna. A drop of 100 mV is necessary to get information of antenna connected.



Antenna sensor connections

ANT_INFO Logic Output Signal

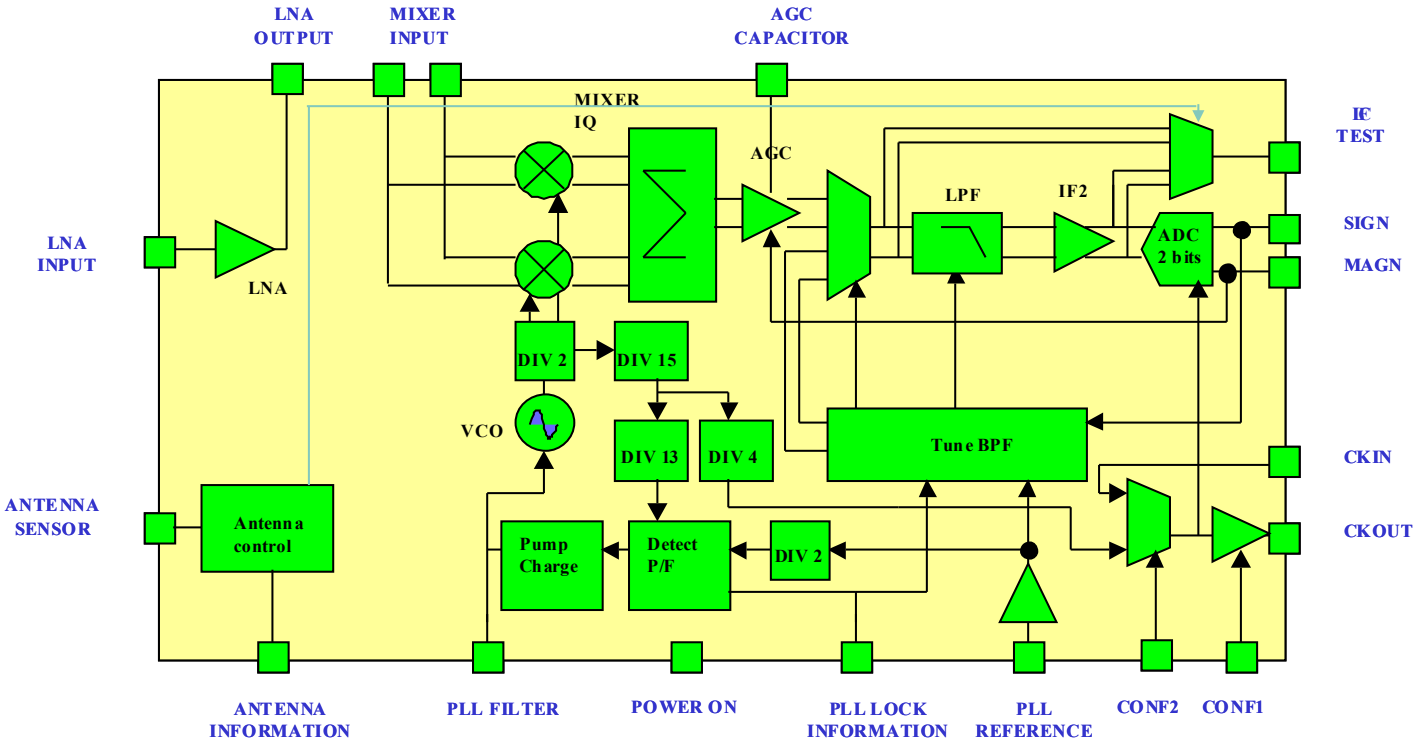
INFORMATION	Logic Level ANT_INFO
Antenna disconnected Antenna connected	0 1

R1 should be set to take in account this internal threshold and the active antenna current consumption. The drop is based on the voltage difference between VCC_LNA and the ANT_SENSE pin.

External components used for the antenna sense

ANT_SENSE pin Voltage	IF_test output selection
> VCC/2 < VCC/2	ADC input AGC output

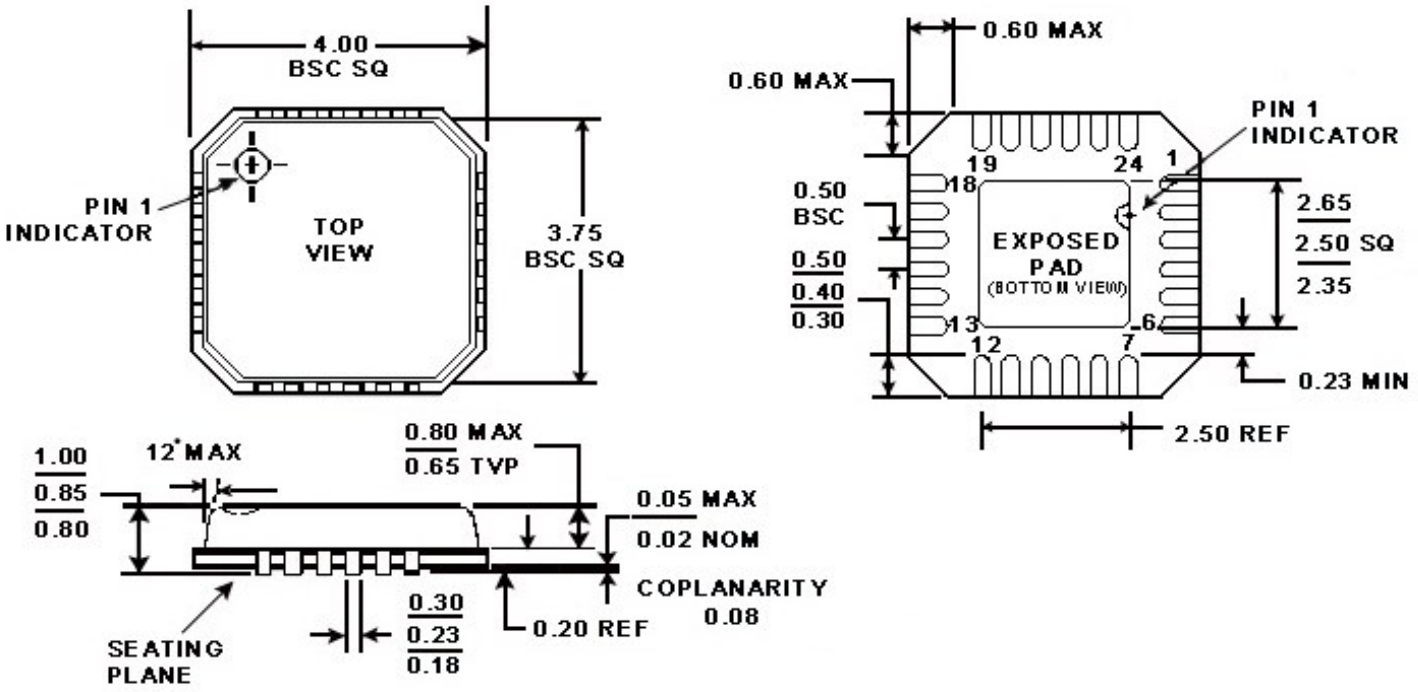
DETAILED BLOCK DIAGRAM



CHIP INFORMATION

Outline Dimensions

24-Lead Lead Frame Chip Scale Package[LFCSP_VQ]
4x4mm Body. Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

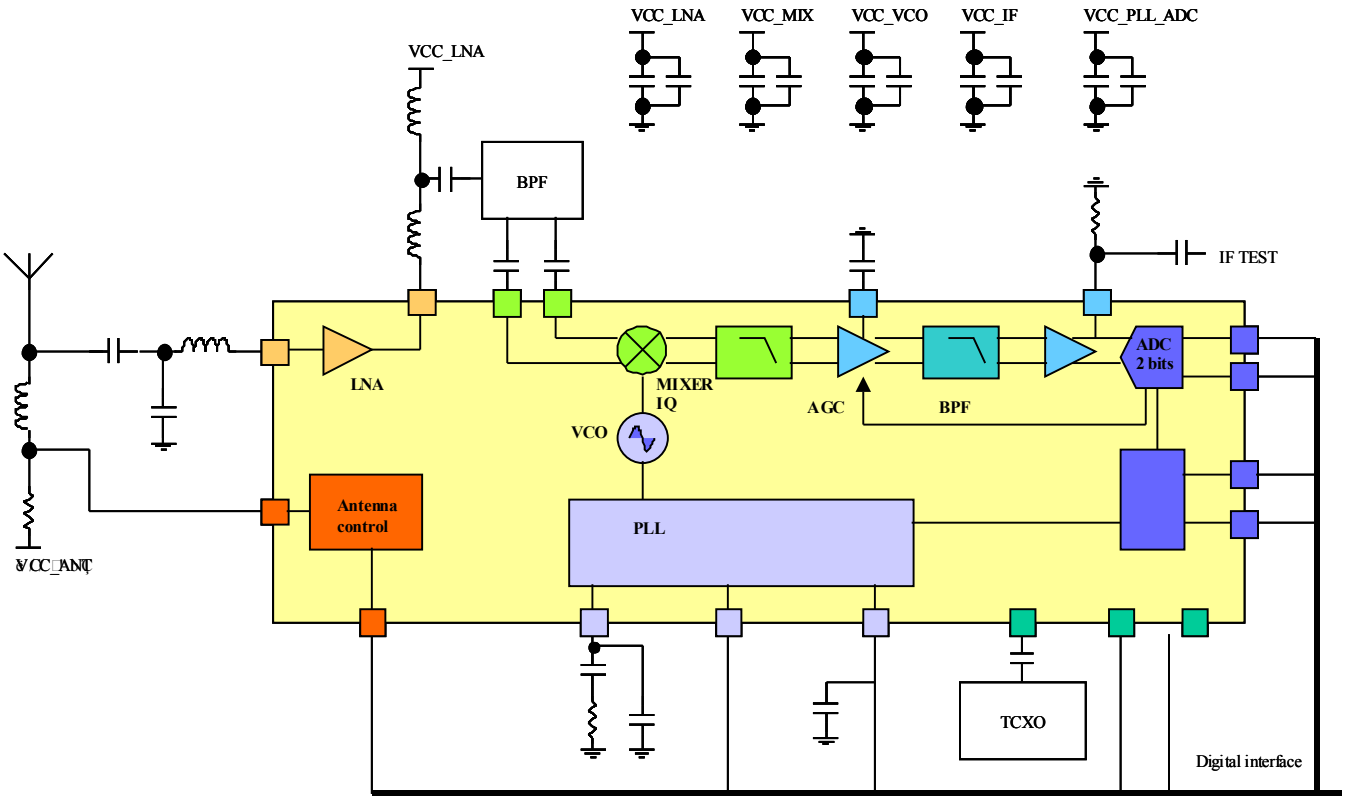


COMPLAINT TO JEDEC STANDARDS MO-220-VGGD-8

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
AST-GLSRF	3.0 V	- 40°C to +85°C	24L LFCSP 4mm x 4mm x 0.85mm Lead Free Package	

APPLICATION SCHEMATIC



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