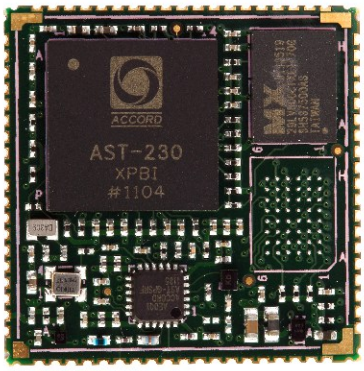
NAVIKA

Navika-110 GPS based Application Engine

Features

- 32-Channel high performance GPS-SBAS Receiver
  - Indoor positioning
  - Fast time to fix
- ARM7 based processing engine
  - 90MHz operating frequency
  - JTAG and Trace support
  - ARM and Thumb mode
- Memory
  - 2Mbit on-chip SRAM
  - 32Kbit battery backed on-chip SRAM
  - 4Mbit SRAM
  - 8Mbit parallel Flash
- Industry standard peripherals
  - USB 2.0 with Full Speed PHY
  - CAN 2.0 controller
  - SPI
  - TWI (I2C compatible)
  - Serial Port
  - UART
  - General Purpose I/O
- Multiple boot mechanisms
- Scalable system clock frequency
- 3.3V I/O
- 1”x 1” PCB with LGA pads
- Fully ROHS compliant



Navika-110
(1”x 1”)

Product Description

Navika-110 is a GPS based application platform designed to host a multitude of applications that need GPS. For an application designer, Navika-110 offers an easy integration option with most of the key system elements already incorporated.

Navika-110 is a 1” x 1” module with LGA pads for assembly. With 76 interface pads, all the relevant power and signal connectivity are brought out of the module.

The GPS block on the Navika-110 is a high performance engine with superior sensitivity and fast fix times.

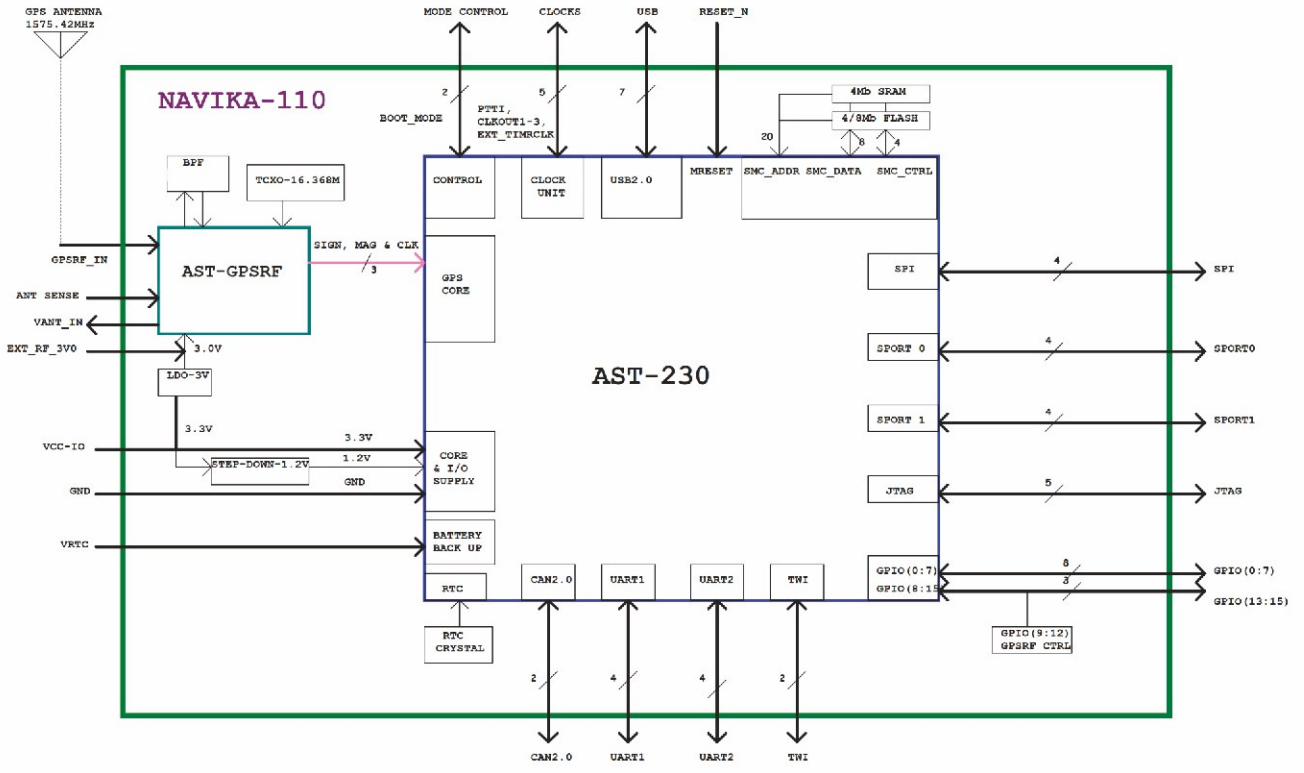
The ARM7 processing core available on the Navika-110 operates at 90MHz and of this, about 50MIPS is available for user applications.

Several real time operating systems are available for the processing core making application development seamless.

Navika-110 brings out the several industry standard peripherals for interface with the external world. USB 2.0 allows the AST-230 to be used for portable applications. CAN 2.0 controller has been integrated to support automotive applications. Other standard peripherals like UART, SPI, TWI and Serial Port provide varied communication interface options. Internal peripherals such as Timers, RTC, Battery backed counter and Watch dog timer provide several options for event based applications.

Navika-110 supports a variety of memories both on and off chip. The on-chip memory of 2Mbits can be used to run application programs at the core frequency. In addition, 32Kbits of the memory is battery backed to facilitate retention of key configuration parameters. External SRAM of 4Mbits can be used to augment the runtime memory capacity while the 8Mbit parallel flash holds the application program.

Navika-110 can be booted in multiple modes offering flexibility for system design. Application program can be stored either in parallel flash that is on-board, or serial flash present off-board or it can be loaded from an external SPI master.

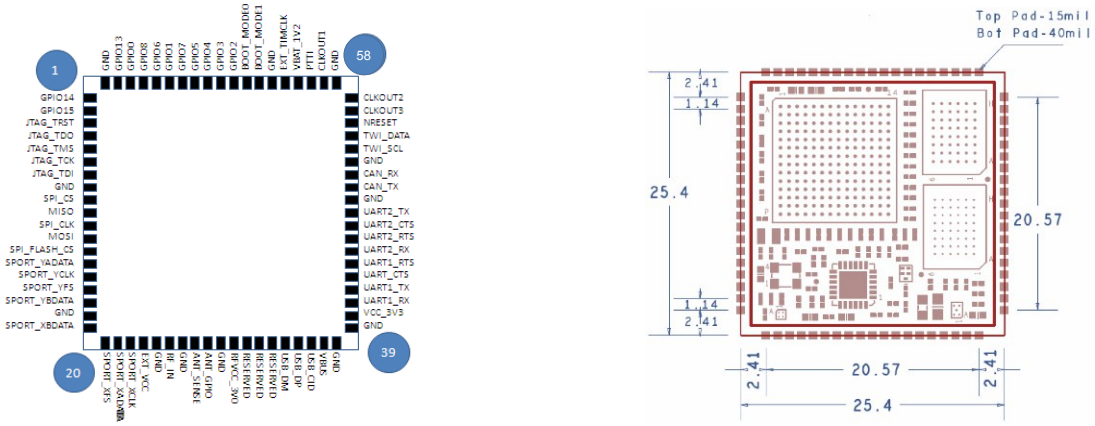


Block Diagram of the Navika-110

Navika-110 consists of AST-GPSRF interfaced with AST-230.

AST-GPSRF is a tiny GPS-SBAS front-end with highly integrated electronics. It has in-built LNA, Mixer, PLL and IF Bandpass filter among other innovative blocks. Antenna connectivity status is also supported on the AST-GPSRF.

AST-230 is a digital System on Chip (SOC) which has the GPS baseband interfaced internally to an ARM7 core. In addition, the AST-230 has several industry standard peripherals such as USB 2.0, CAN 2.0, GPIO, UART, SPI, TWI, SPORT, Timers, Watchdog timer, Static Memory Controller etc. The chip has internal 2Mbit SRAM which allows the user application along with GPS algorithms to run on the same memory.



Mechanical Details of the Navika-110

Performance Specifications of Navika-110

Time to First Fix

Hot Start (with valid ephemeris, almanac, position and time estimate)	:2-3 sec (typical) switch OFF/ON cycle less than 1 hour
Warm Start(with almanac, position and time estimate)	:30 sec (typical)
Cold Start (without almanac, time, or position)	:35 sec (typical)

Note: Active antenna kept under open sky with HDOP<2 and C/N0 > 40dB-Hz

Accuracy

Position (Horizontal)	:<2.5m (RMS)
Velocity	:0.1 m/sec (90% without S/A)

Note: Active antenna kept under open sky with HDOP<2 and C/N0 > 40dB-Hz

Timing

1PPS	: < +/- 10ns, RMS without errors
Pulse Width	: 386us (adjustable between 386us to 500ms in steps of 386us)
Pulse Edge	: Rising (configurable)
Pulse Delay	: 0ns (adjustable between –999 to +999ns)

Environmental Characteristics

Operational Temperature Range (Ambient)	:-40°C to +85°C
Storage Temperature Range	:-65°C to +150°C
Humidity	:95% non-condensing +30°C to 60°C
Altitude	:18,000 meters

Electrical Characteristics

Total Current Consumption	:85mA @ 3.3V
GPS MIPS on ARM	:25

General Specifications of Navika-110

GPS-SBAS

Acquisition Channels	: 16
Tracking Channels	: 16
Acquisition Sensitivity	: -160 dBm
Tracking Sensitivity	: -163 dBm
Power consumption	: 150 mW

PROCESSING CORE – ARM7

Operating frequency	: 90 MHz
Bus architecture	: AMBA Standard – AHB and APB
AHB frequency	: 90 MHz (max)
APB frequency	: 45 MHz (max)
Instruction set	: ARM and Thumb modes
Power consumption	: 90mW

USB

PHY	: Full speed
Characteristics	: Device
Communication Interface	: VCC, GND, D+, D-

CAN

Specification	: CAN 2.0
Mailboxes	: 16 for objects of 8-bytes data length4 Transmit-only, 4 Receive-only, 8 Transmit-Receive
Remote frames	: Extended data and remote frame support
Communication Interface	: CAN Tx and Rx

SPI

System Clock	: 22.5 MHz (max)
Slave select	: 6
Chip select	: 1
Modes	: Master, Slave, Multi-master, Boot
Interrupt	: Supported
DMA	: Supported

TWO WIRE INTERFACE (TWI)

System Clock	: 400 Khz
Modes	: Master, Slave, Multi-master
Interrupt	: Supported

General Specifications of Navika-110

SERIAL PORT (SPORT)

System Clock	: 22.5 MHz
Clock source	: Internally generated or External source
Word length	: 3 to 32 bits, big or little endian
Framing	: Supported
Interrupt	: Supported
I2S	: Supported
Multi-channel capability	: Supported
Availability	: 2 SPORT's, configurable as full-duplex

UART

Speed of operation	: Upto 1 Mbps
Type	: Full UART with frame control
Word length	: 7 to 12 bits
Interrupt	: Supported
DMA	: Supported
Availability	: 2 UART's

GPIO

Available ports	: 12 bi-directional; configurable as either input or output
Interrupt	: Supported

TIMER

Available	: 3
External clock input	: Supported
Interrupt	: Supported

REAL TIME CLOCK (RTC)

Mode	: 32-bit free running counter
Clock	: 32.768 KHz crystal
Power down / wake up features	: Supported

WATCH DOG TIMER (WDT)

Mode	: 32-bit counter; programmable through software
Clock	: 32.768 KHz crystal
Configuration	: Core and Peripheral reset upon expiry of counter
Traceability	: Sticky bit to indicate if reset happened due to Watch Dog function

CLOCKS

System Clock	: 90 MHZ (max)
Peripheral Clock	: 45 MHZ (max)
Battery backed peripherals	: 32.768 KHz

RESET

Reset	:Active Low Chip Reset input, at least 25 ms low pulse

JTAG

JTAG	: TDO, TDI, TCK, TMS and TRST lines

MECHANICAL

Dimensions	: 1" x 1"
Pads	: 76 LGA with edge plated connection points

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