# Navika-111
# High Performance GPS-GSM Combo module

## Datasheet

## Document History

| Sl No. | Version | Changed By | Changed On | Change Description |
|---|---|---|---|---|
| 1 | 0.1 | Sudhir N S | 13-09-2014 | Created |

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# Introduction

Navika-111 is a versatile platform that integrates two key sensors - GPS and GSM - on a single board. It is targeted towards varied applications such as vehicle tracking, auto fare meters, handheld terminals etc. Navika-111 simplifies the whole concept of product design by sucking in the major elements onto itself, thereby freeing up valuable design time for the customer. In addition to the key sensors, Navika-111 provides a processing platform that allows user applications to run concurrently with the core sensor libraries. Availability of a comprehensive board support package with device drivers and elaborate documentation, Navika-111 eases the product design life cycle. Navika-111 provides additional features such as a fully functional Bluetooth module and an FM module to add to the value proposition. With this, customers can plan for a range of scalable products keeping Navika-111 at the heart.

This document provides detailed information on the Navika-111 and is organized into the following chapters –

| | | |
|---|---|---|
| Chapter 1 | Product Description | Describes –<br>• Product description<br>• Block diagram<br>• Features |
| Chapter 2 | Hardware Details | Describes –<br>• Mechanical details<br>• Pinouts<br>• Recommended and application circuits |
| Chapter 3 | Specifications | Describes –<br>• Performance specification<br>• Electrical specification<br>• Environmental specification<br>• Qualification and certification |
| Chapter 4 | Assembly Instructions | Describes –<br>• Packaging<br>• Shipment<br>• Storage<br>• Handling<br>• Soldering<br>• Testing |
| Chapter 5 | Ordering Information | Describes –<br>• Ordering |

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## Scope

The scope of this document is to present the salient features of the Navika-111 GPS-SBAS application platform. It in no way implies that the information shared is recommended for the end application. The schematic and BOM is shared for the basis of providing information about the hardware circuitry. It in no way recommends the use of identical circuit and / or components in the customer application hardware.

## Audience

The audience for this document is hardware and application engineers who would be interested in using the Navika-111 in their end applications.

## Support

Support for the Navika-111 is available through the following ways –

- Email questions to
  - Gnss_faq@navikaelectronics.com
- Phone questions to
  - +91-80-25350105 extn 233
- Fax questions to
  - +91-80-25352723
- Snail mail questions to

- Navika Electronics
  37, Krishna Reddy Colony,
  Domlur Layout
  Bangalore – 560071
  INDIA

## Related Documents

In addition, a system integrator would need to refer to additional resources to gain complete information about the Navika-111 hardware and software features.

These are listed below –

| Resource | Description | Availability |
|---|---|---|
| AST-GPSRF Datasheet | The datasheet contains the detailed description and specifications of the AST-GPSRF front-end | www.navika-electronics.com |
| AST-230 Datasheet | The datasheet contains the detailed description and specifications of the AST-230 digital baseband | www.navika-electronics.com |
| AST-230 Programmer's Manual | The programmer's manual contains the detailed description of each and every functional block of the AST-230 and their programming registers | www.navika-electronics.com |
| AST-230 Software Integration Plan Document | The integration plan describes the way to combine an application software module with GPS library on the AST-230 | www.navika-electronics.com |
| AST-230 Anomaly Listing | The anomaly listing document lists the anomalies in the current version of the AST-230 chip and the possible work-arounds | www.navika-electronics.com |
| Navika GNSS Message Details | The message details contains the list of input and output messages supported by the GPS firmware when running on the Navika-111 | www.navika-electronics.com |
| SIM800H Specifications<br>SIM800H AT commands<br>SIM800H Bluetooth Application Note V1.01<br>SIM800H FM Application Note V1.0<br>SIM800H Hardware Design V1.0 | The GSM modem used on the Navika-111 is SIM800H from Simcom. The module specifications can be obtained from Simcom website | www.sim.com |

# Chapter 1: Product Description

## *Overview*

Navika-111 is a versatile application module with GPS and GSM/GPRS functionality. It integrates a GPS RF front-end, GPS baseband, ARM7 based application processor and a GSM/GPRS module on a space saving PCB. With 92 connection pads all around the PCB, Navika-111 brings out the antenna, signal and power connections for easy access. In addition to GPS and GSM, Navika-111 also supports Bluetooth and FM with their respective antenna feeds.

The GPS section of the Navika-111 is a high performance module with key performance figures such as 2-3s Hot start TTFF, -162dBm Tracking Sensitivity, Position accuracy of 2.5m and all-in-view positioning. Navika-111 is ideally suited for applications that demand superior performance from the GPS sensor.

Navika-111 integrates a miniature and highly integrated GSM modem. The modem supports quad-band operation, GPRS multi-slot class 12/10, compliant to GSM phase 2/2+ class 4 and 1 and voice function among other features.

For applications that require a short range connectivity, Navika-111 also includes a full function Bluetooth 3.0+ EDR.

Additionally, Navika-111 also supports FM over 76MHz to 109MHz worldwide bands.

Navika-111 also supports a variety of memories both on and off chip. The on-chip memory of 2Mbits can be used to run application programs at the core frequency of 90MHz. In addition, 32Kbits of the memory is battery backed to facilitate retention of key configuration parameters. The on-board SRAM of 4Mbits can be used to augment the runtime memory capacity while the 8Mbit parallel flash holds the application program.

Navika-111 brings out the several industry standard peripherals for interface with the external world. USB 2.0 full speed PHY to allow bulk data transfers between the Navika-111 and a host. CAN 2.0 controller has been integrated to support automotive applications. Other standard peripherals like UART, SPI, TWI and Serial Port provide varied communication interface options. Internal peripherals such as Timers, RTC, Battery backed counter and Watch dog timer provide several options for event based applications. In addition, Navika-111 provides a 10-bit single channel ADC to process analog inputs. It also brings out a frequency counter port to interface with vehicle odometers.

In order to enable seamless usage of the Navika-111 into various applications, Navika-111 module is supplemented with a software package which consists of a comprehensive board support package, device drivers and application libraries. Customers can build on the software package to add their own applications to run on the Navika-111.

## *Block Diagram*

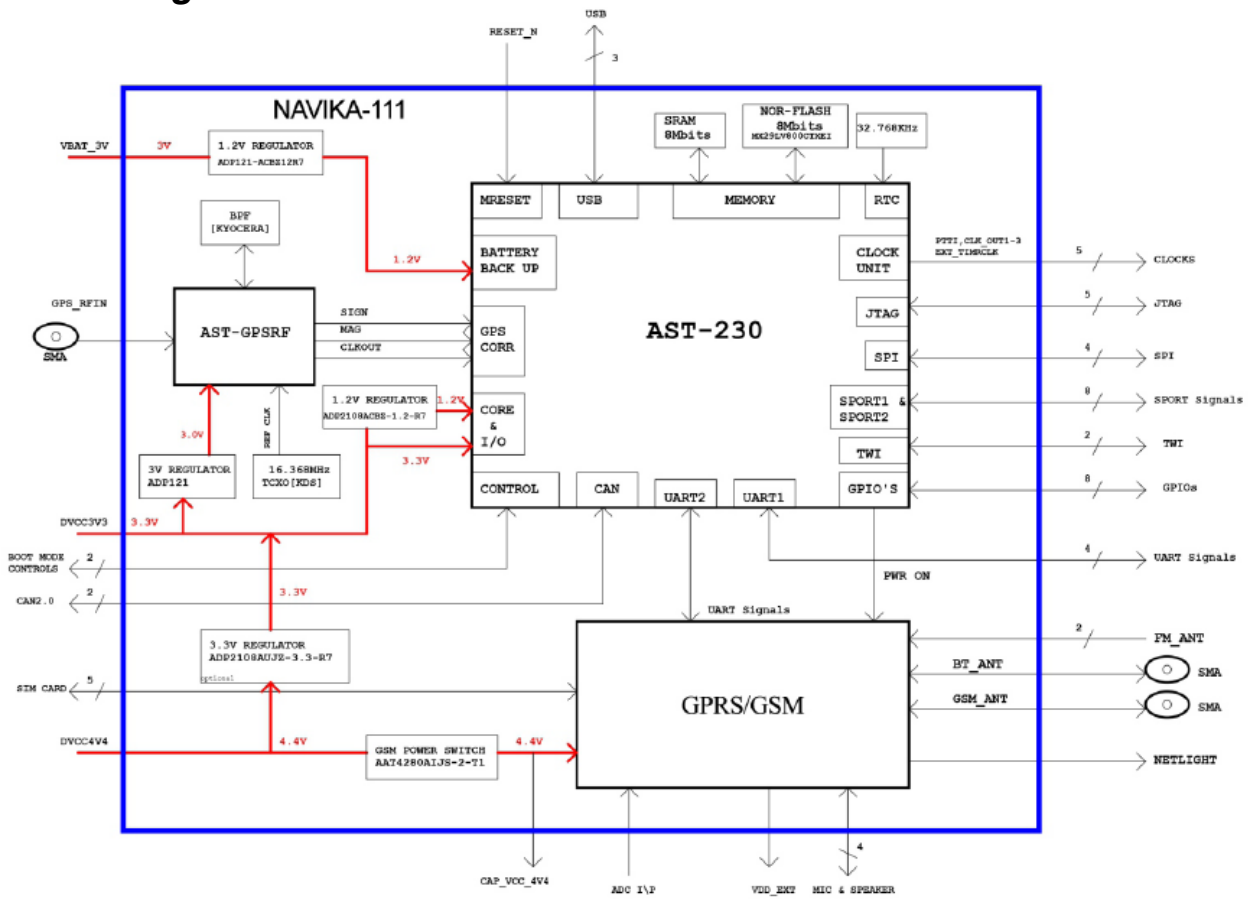



Figure 1: Block Diagram of Navika-111

## *Features*

| Feature | Description |
|---|---|
| GPS-SBAS | Supports a 32-channel GPS-SBAS receiver with 16 channels each for acquisition and tracking |
| GSM/GPRS | Supports a quad-band modem for SMS and GPRS communication along with voice capability |
| Bluetooth | Supports Bluetooth 3.0+ EDR |
| FM | Supports global wide FM frequencies |
| AGPS | Supports AGPS data input when interfaced to a cellular network through a GSM-GPRS modem |
| Navigation solution | Outputs position, velocity and time either over the UART or USB or as API for internal data exchange between GPS and user application |
| 1PPS | Provides a precise 1PPS pulse output synchronized to GPS / UTC time standard |
| Antenna interface | Supports both active and passive antenna |
| Antenna monitoring | Active antenna open or short circuit detection and protection<br>This requires an external resistor to be provisioned |
| Output protocol | Standard NMEA 0183 v3.0<br>Accord binary<br>Accord ASCII<br>RINEX message format |
| Input protocol | Accord ASCII |
| Small footprint | Navika-111 is available in a small 50mm x 26mm 4.0mm form factor |
| Memory | • On-chip 2Mbit SRAM<br>• On-chip 32Kbit battery backed SRAM<br>• On-board 4 Mbit of SRAM<br>• On-board 8 Mbit of Parallel flash |
| Peripherals | • USB 2.0 Full Speed<br>• SPI<br>• UART<br>• General Purpose I/O (GPIO)<br>• CAN 2.0 controller<br>• TWI (I2C compatible)<br>• Serial ports<br>• Time and Frequency output |

| | |
|---|---|
| | • ADC<br>• PWM output<br>• Frequency Counter |
| Power supply | Navika-111 operates out of three power domains –<br>• 3.3V I/O, GPS<br>• 4.4V GSM/GPRS<br>• 3.0V battery backup |

Table 1: Feature list of Navika-111

# Chapter 2: Hardware Details

This chapter describes the mechanical details, pin outs and recommended circuits to use the Navika-111 module and its hardware interfaces.

## *Mechanical Details*

Navika-111 is a 50mm x 26mm x 4.0mm GPS-GSM module. The mechanical details are shown in the figure below.

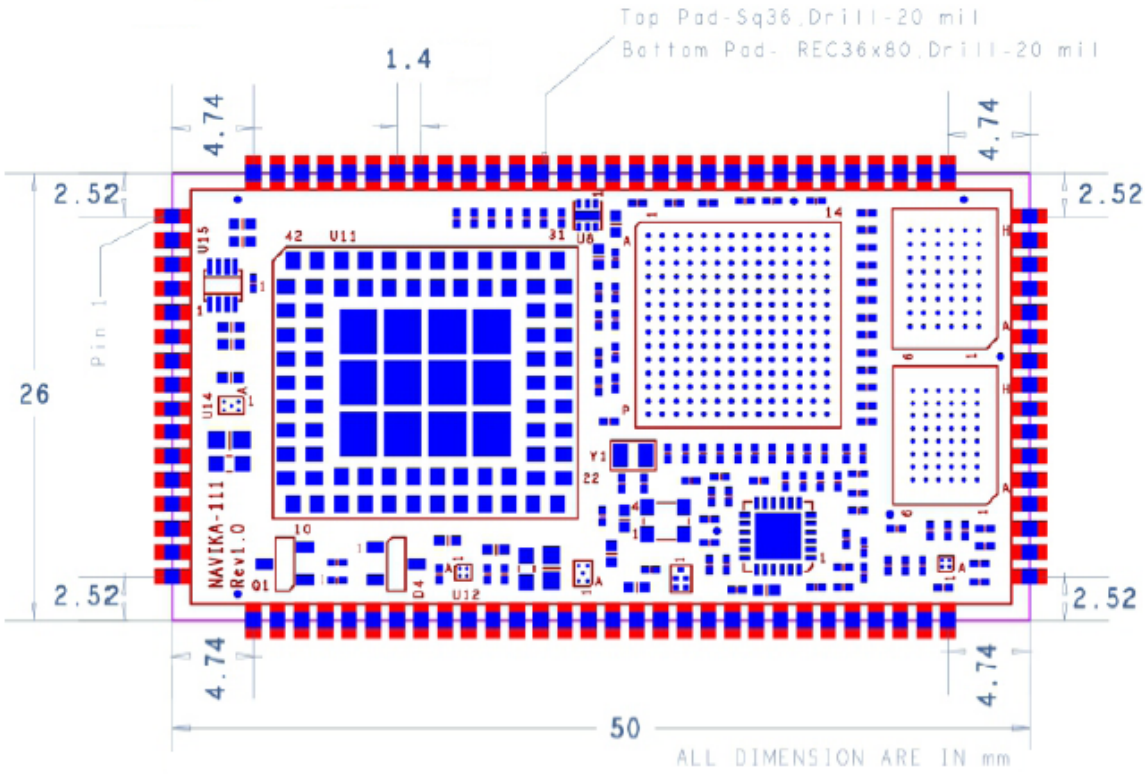



*Figure 2: Navika-111 Package outline and dimensions*

## *Pin outs*

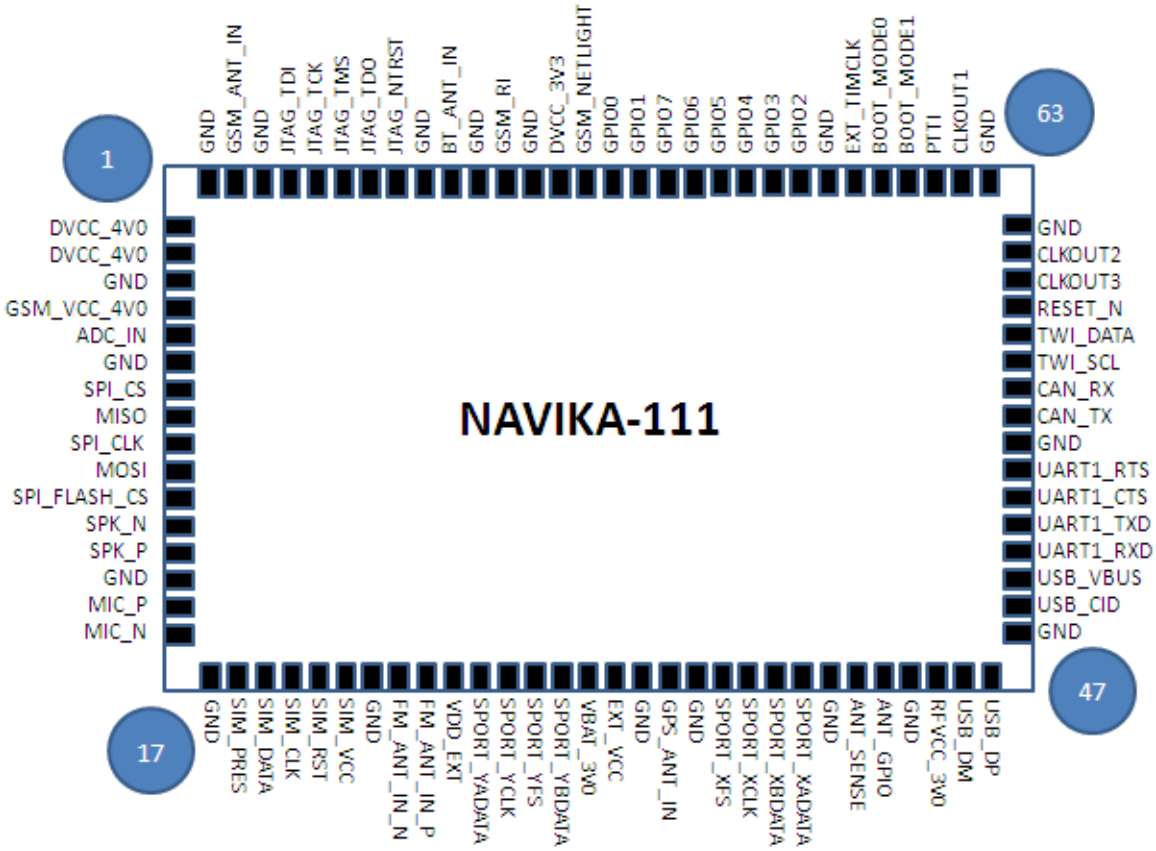



*Figure 3: Navika-111 Pin outs*

The table below provides the pin definition and the description / specification of each pin.

| Pin Number | Pin Name | Input / Output | Description | Pull up /Pull down / Comments |
|---|---|---|---|---|
| 1, 2 | DVCC_4V0 | | Power supply input for the entire module | See Power Supply section for more details |
| 3 | GND | | Ground | |
| 4 | GSM_VCC_4V0 | | Pad to supply additional capacitance for the GSM modem | See Power Supply section for more details |
| 5 | ADC_IN | I | Analog signal input to the on-board ADC | |
| 6 | GND | | Ground | |
| 7 | SPI_CS | I | SPI chip select | Pull up |
| 8 | MISO | I | SPI MISO | Pull up |
| 9 | SPI_CLK | O | SPI clock | |
| 10 | MOSI | O | SPI MOSI | Pull up |
| 11 | SPI_FLASH_CS | O | SPI Flash chip select | Pull up |
| 12 | SPK_N | O | Differential audio output | Recommended circuit given under GSM Section |
| 13 | SPK_P | O | Differential audio output | Recommended circuit given under GSM Section |
| 14 | GND | | Ground | |
| 15 | MIC_P | I | Differential audio input | Recommended circuit given under GSM Section |
| 16 | MIC_N | I | Differential audio input | Recommended circuit given under GSM Section |
| 17 | GND | | Ground | |
| 18 | SIM_PRES | I | SIM Card Detection | Protect with TVS diode against ESD |
| 19 | SIM_DATA | I/O | SIM Data input and output | Protect with TVS diode against ESD |
| 20 | SIM_CLK | O | SIM Clock | Protect with TVS |

| | | | | |
|---|---|---|---|---|
| | | | | diode against ESD |
| 21 | SIM_RST | O | SIM Reset | Protect with TVS diode against ESD |
| 22 | SIM_VCC | O | Supply voltage for SIM card. Supports both 1.8V and 3V SIM cards | Protect with TVS diode against ESD |
| 23 | GND | | Ground | |
| 24 | FM_ANT_IN_N | I | Differential antenna input for FM | Recommended circuit given under FM Section |
| 25 | FM_ANT_IN_P | I | Differential antenna input for FM | Recommended circuit given under FM Section |
| 26 | DVCC_2V8 | O | 2.8V supply output from the module | See Power Supply section for more details |
| 27 | SPORT_YADATA | I/O | SPORT Y-channel A Data | Pull down |
| 28 | SPORT_YCLK | I/O | SPORT Y-channel clock | Pull down |
| 29 | SPORT_YFS | I/O | Frame sync for Y-channel | Pull down |
| 30 | SPORT_YBDATA | I/O | SPORT Y-channel B Data | Pull down |
| 31 | VBAT_3V0 | I | Battery domain supply | |
| 32 | EXT_VCC | I | Supply for antenna | |
| 33 | GND | | Ground | |
| 34 | GPS_ANT_IN | I | RF input | 50 ohm impedance trace be to implemented on the PCB |
| 35 | GND | | Ground | |
| 36 | SPORT_XFS | I/O | Frame sync for X-channel | Pull down |
| 37 | SPORT_XCLK | I/O | SPORT X-channel clock | Pull down |
| 38 | SPORT_XBDATA | I/O | SPORT X-channel B Data | Pull down |
| 39 | SPORT_XADATA | I/O | SPORT X-channel A Data | Pull down |
| 40 | GND | | Ground | |
| 41 | ANT_SENSE | I | Antenna detect input | |
| 42 | ANT_GPIO | I/O | Antenna status indication | |

| | | | | |
|---|---|---|---|---|
| 43 | Gnd | | Ground | |
| 44 | RFVCC_3V0 | O | Supply voltage for active GPS antenna generated by the module | |
| 45 | USB_DM | I/O | USB D+ line | |
| 46 | USB_DP | I/O | USB D- line | |
| 47 | GND | | Ground | |
| 48 | USB_CID | I/O | Device ID detection input pin | |
| 49 | USB_VBUS | I/O | VBUS input | |
| 50 | UART1_RXD | I | UART1 Receive | Pull up |
| 51 | UART1_TXD | O | UART1 Transmit | |
| 52 | UART1_CTS | I | UART1 Clear to send | |
| 53 | UART1_RTS | O | UART1 Request to send | |
| 54 | GND | | Ground | |
| 55 | CAN_TX | O | CAN controller Tx Data out | |
| 56 | CAN_RX | I | CAN controller Rx Data in | |
| 57 | TWI_SCL | I/O | I2C serial clock | Pull up |
| 58 | TWI_DATA | I/O | I2C Data pin | Pull up |
| 59 | RESET_N | I | Master reset input | Pull up |
| 60 | CLKOUT3 | O | Programmable clock O/P | |
| 61 | CLKOUT2 | O | Programmable clock O/P | |
| 62 | GND | | Ground | |
| 63 | GND | | Ground | |
| 64 | CLKOUT1 | O | Programmable clock O/P | |
| 65 | PTTI | O | Precise one second pulse | |
| 66 | BOOT_MODE1 | I | Boot mode selection pin | |
| 67 | BOOT_MODE0 | I | Boot mode selection pin | |
| 68 | EXT_TIMCLK | I | External timer clock input | |
| 69 | GND | | Ground | |
| 70 | GPIO2 | I/O | General purpose I/O | |
| 71 | GPIO3 | I/O | General purpose I/O | |
| 72 | GPIO4 | I/O | General purpose I/O | |
| 73 | GPIO5 | I/O | General purpose I/O | |
| 74 | GPIO6 | I/O | General purpose I/O | |
| 75 | GPIO7 | I/O | General purpose I/O | |

| | | | | |
|---|---|---|---|---|
| 76 | GPIO1 | I/O | General purpose I/O | |
| 77 | GPIO0 | I/O | General purpose I/O | |
| 78 | GSM_NETLIGHT | O | Network registration status of GSM | |
| 79 | DVCC_3V3 | O | 3.3V supply output from the module | See Power Supply section for more details |
| 80 | GND | | Ground | |
| 81 | GSM_RI | O | GSM Ring Indicator | |
| 82 | GND | | Ground | |
| 83 | BT_ANT_IN | | Bluetooth antenna input | Recommended circuit given under Bluetooth Section |
| 84 | GND | | Ground | |
| 85 | JTAG_NTRST | I | JTAG RESET | Pull up |
| 86 | JTAG_TDO | O | JTAG Data Out | |
| 87 | JTAG_TMS | I | JTAG Mode select i/p | |
| 88 | JTAG_TCK | I | JTAG clock | Pull up |
| 89 | JTAG_TDI | I | JTAG Data i/p | Pull up |
| 90 | GND | | Ground | |
| 91 | GSM_ANT_IN | | GSM antenna input | Recommended circuit given under GSM Section |
| 92 | GND | | Ground | |

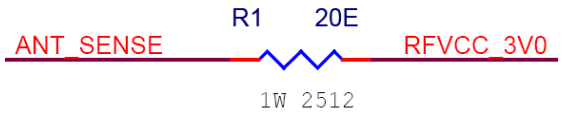
Table 2: Navika-111 pin details and recommended terminations

## *Key Hardware Blocks*

This section describes the key hardware blocks and interfaces of the Navika-111. The block diagram shown in Figure 1 earlier is a good starting point to understand the Navika-111 hardware architecture. As seen, the core building blocks of the Navika-111 are the GPS RF section, GSM section, Bluetooth section, FM section, the digital baseband section, peripherals, memory and power supply. The interfaces are brought out of the module through edge castellations.

### GPS Section

The Navika-111 provides a select choice of signal and power pins corresponding to the GPS RF section. These are tabulated below.

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 32 | EXT_VCC | External antenna supply can be provided on this pin. |
| 34 | GPS_ANT_IN | The antenna output should be brought to this pad through a 50 ohm matching trace on the PCB. The bias voltage to the active antenna is supplied by the module itself. This is explained under ANT_SENSE pin description. |
| 41 | ANT_SENSE | This pad accepts the antenna bias voltage as an input to decide if the active antenna is connected or has been short circuited. A typical connection is shown below. The 20 ohm resistor is used to prevent excessive current flow in the event of the antenna getting short circuited.<br>If a passive antenna is to be interfaced to the Navika-111, R1 should be left open.<br>The below circuit is not recommended if external antenna bias voltage is to be fed to the antenna.<br>  |
| 42 | ANT_GPIO | If an external antenna short circuit protection circuitry is employed and a status line is required to indicate the status of the antenna, the same can be connected to this pin. The voltage level to be fed should be CMOS (0 to 3.3V). Otherwise, leave this pin open. |
| 44 | RFVCC_3V0 | Supply voltage of 3.0V +/- 5% available from the module as antenna bias voltage. See ANT_SENSE for more information. The maximum current that can be sourced from this pin is 50mA. |

### GPS Antenna

The GPS section of the Navika-111 supports an active GPS antenna and as such a pad is provisioned to interface to such an antenna.

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 91 | GPS_ANT_IN | A 50 ohm trace should be routed between the pad and the GPS antenna. |

As all matching components are incorporated on the Navika-111 module itself, all it takes to implement the GPS antenna interface is to design in a suitable connector and draw a 50 ohm trace between the connector and the GPS_ANT_IN pad.

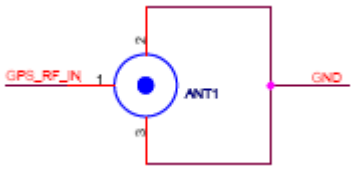



*Figure 4: GPS antenna circuit*

## GSM Section

The following table lists the various signal and power pads corresponding to the GSM section of the Navika-111.

### Speaker

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 12, 13 | SPK_N, SPK_P | The differential Speaker output lines can directly drive a 32 ohm load. |

A recommended circuit is shown below.

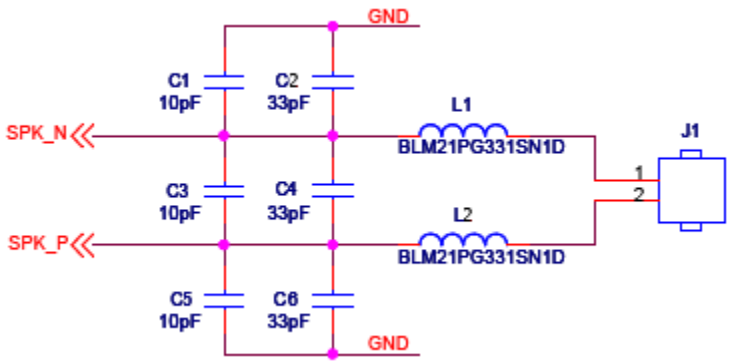


*Figure 5: Speaker circuit*

**Microphone**

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 15, 16 | MIC_P, MIC_N | The differential Microphone input lines can be driven by an electret microphone.<br>A recommended circuit is shown below. |

A recommended circuit is shown below.

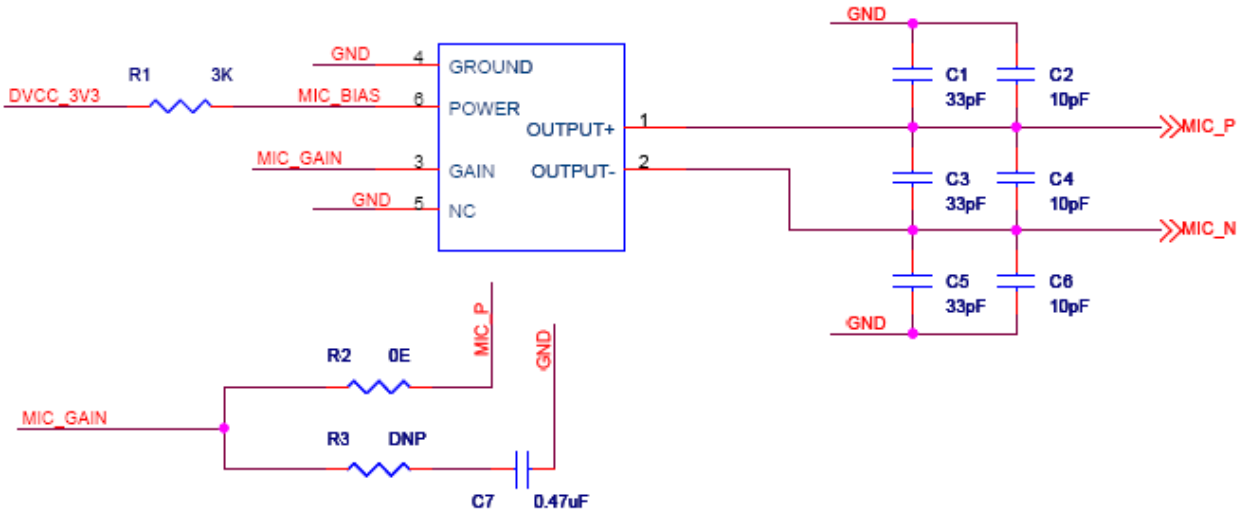



*Figure 6: Microphone circuit*

**SIM Card**

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 18 | SIM_PRES | Useful for hot plug-in of SIM card.<br>Valid for a 8-pin SIM card |
| 19 | SIM_DATA | Valid for both 6-pin and 8-pin SIM card |
| 20 | SIM_CLK | Valid for both 6-pin and 8-pin SIM card |
| 21 | SIM_RST | Valid for both 6-pin and 8-pin SIM card |
| 22 | SIM_VCC | Valid for both 6-pin and 8-pin SIM card |

The SIM interface pins provided can support a 8-Pin SIM or a 6-Pin SIM. The SIM_PRES pad allows hot plug in of the SIM card and is supported by an AT command to enable or disable the feature.

The below circuit shows the recommended circuit for a 6-pin SIM card along with the ESD diodes.

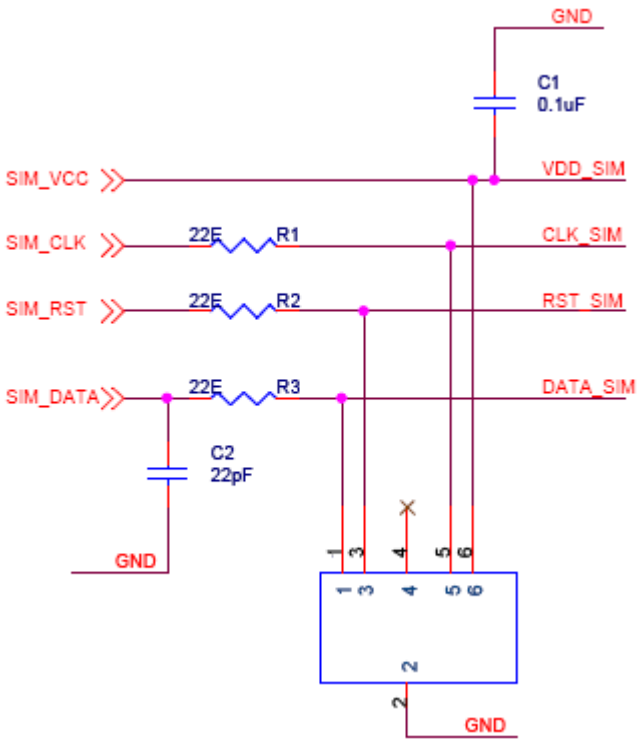



*Figure 7: SIM card connection details*

**GSM Netlight**

The Netlight pad indicates the status of the network registration status. It is typically used to drive a LED and the rate at which the LED turns ON and OFF is an indication of the status.

The table below provides the mapping for the blink rate and the status.

| LED Blink Rate | GSM Network Registration Status |
|---|---|
| OFF | GSM section not ON / not working |
| 64ms ON / 800ms OFF | GSM section not registered to the network |
| 64ms ON / 3000ms OFF | GSM section registered to the network |
| 64ms ON / 300ms OFF | GPRS communication established |

Recommended circuit for the Netlight pad to drive an LED is shown below.

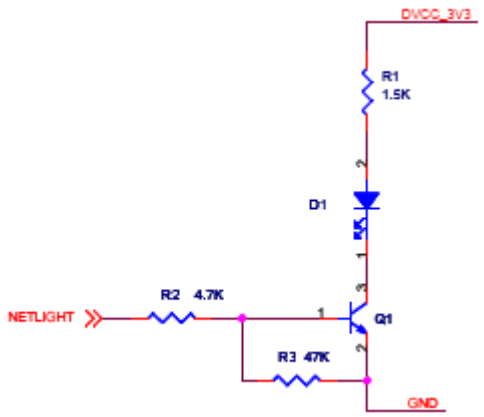



*Figure 8: Network Status Indication circuit*

**GSM Ring Indicator**

| Pad identification | Signal / Power name | Status |
|---|---|---|
| 81 | GSM_RI | Default: High<br>Voice call: Low upon receiving a call and high once the call is established or the call is hung<br>Data call: Low upon receiving a call and high once the call is established or the call is hung<br>SMS: Low for a period of 120ms when an SMS is received and high soon after |

**GSM Antenna**

The GSM section of the Navika-111 provides a pad for GSM antenna connection. This has to be AC coupled and should have a provision for a matching network in the event the antenna is not properly matched to the modules antenna port.

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 91 | GSM_ANT_IN | A 50 ohm trace should be routed between the pad and the GSM antenna. It may be necessary to match the antenna with the module antenna port and it is recommended to follow the below circuit |

A recommended circuit for the GSM antenna is given below. The values of R1, C1 and C2 can be designed keeping in mind the antenna chosen. Typically, R1 can be 0e while C1 and C2 need not be mounted.

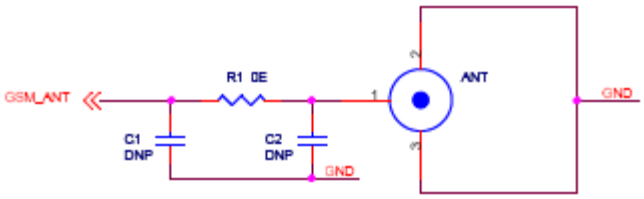



*Figure 9: GSM Antenna circuit*

## Bluetooth Section

The Navika-111 includes a Bluetooth section with integrated RF and baseband. The only external interface required is that of an antenna.

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 83 | BT_ANT_IN | A 50 ohm trace should be routed between the pad and the Bluetooth antenna. It may be necessary to match the antenna with the module antenna port and it is recommended to follow the below circuit |

A recommended circuit for the Bluetooth antenna is given below. The values of R1, C1 and C2 can be designed keeping in mind the antenna chosen. Typically, R1 can be 0e while C1 and C2 need not be mounted.

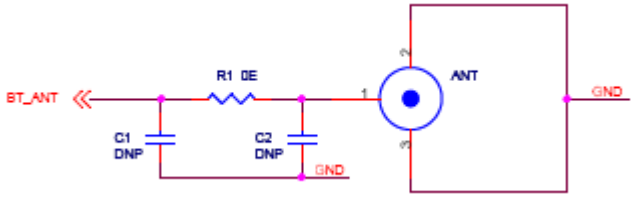



*Figure 10: Bluetooth Antenna circuit*

## FM Section

The Navika-111 includes a FM section with integrated RF and baseband. The only external interface required is that of an antenna to be connected over a differential pair.

| Pad identification | Signal / Power name | Connection Detail |
|---|---|---|
| 25, 26 | FM_ANT_IN_P, FM_ANT_IN_N | A 50 ohm trace should be routed between the pad and the Bluetooth antenna. It may be necessary to match the antenna with the module antenna port and it is recommended to follow the below circuit |

A recommended circuit to make use of the FM feature is given below. Here, the ear phone itself acts as the FM antenna. As shown below, the ground of a 3.5mm earphone is used to interface with the FM antenna pads of the Navika-111 module. Typically, R1 and R2 can be 0e while C1, C2, C3, C4 and L1 need not be mounted.

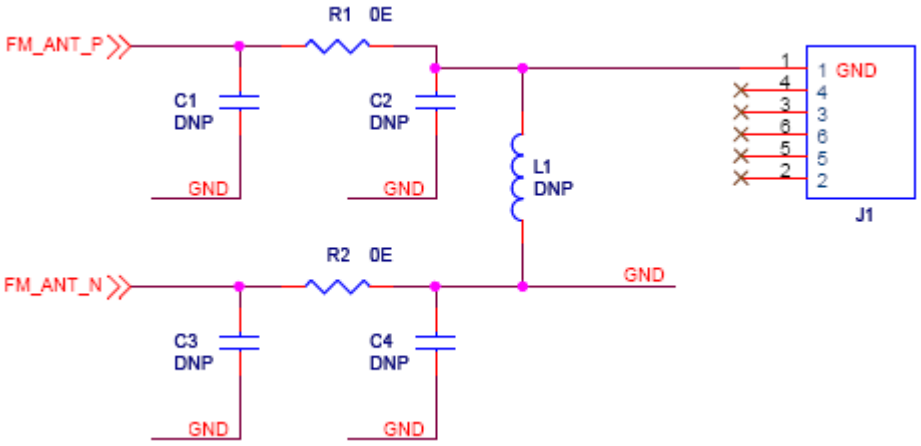



*Figure 11: FM Antenna circuit*

## ARM Subsystem

The ARM subsystem on the Navika-111 consists of the following –

- AST-230 (ARM7 TDMI) processor capable of running at 90MHz (refer to the AST-230 programmer's manual for details)
- Boot Modes
- JTAG

### Boot Modes

The Navika-111 contains multiple boot controllers and provides flexibility in system design. After a reset, the appropriate boot controller loads the firmware into the internal memory at address 0x00000000 and the execution is initiated.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 66 | Boot_mode_1 | Upper of the two boot mode select lines, can be pulled-up or pulled-down to DVCC_3V3 through 4.7K Ohm resistors based on the required boot mode. |
| 67 | Boot_mode_0 | Lower of the two boot mode select lines, can be pulled-up or pulled-down to DVCC_3V3 through 4.7K Ohm resistors based on the required boot mode. |

The boot mode is selected using 2 boot mode pins according to the table below –

| Boot Mode [1:0] | Description |
|---|---|
| 00 | Boot from external Master through SPI interface. |
| 01 | Boot from external Serial Flash. |
| 10 | Boot on-board 16-bit parallel flash. |
| 11 | Reserved. |

The explanation of the different boot modes is as below –

- Boot from Master – In this mode, Navika-111 is connected to a master processor through the SPI interface. Navika-111 is configured as a SPI slave. By implementing a boot protocol, the Navika-111 can be booted from the master processor directly into the internal memory of the AST-230. Once the booting process is complete, AST-230 on the Navika-111 will start execution.

- Boot from Serial Flash – In this mode, an external off-board serial flash is connected over the SPI interface. Navika-111 provides a dedicated chip select (SPI_FLASH_CS, pin 13) for this purpose. The boot controller on the AST-230 controls the SPI port as a master.

- Boot from Parallel Flash – In this mode, AST-230 on the Navika-111 will boot from its on-chip 16-bit parallel flash

For each of the above boot modes, the appropriate controller reads a header. The header contains further information such as bytes to be transferred and destination address. The boot protocol is available as part of AST-230 Programmer's Manual.

**JTAG**

The ARM7 core of the AST-230 on the Navika-111 can be accessed through the standard JTAG. JTAG has 5 pins as listed below.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 85 | JTAG_NTRST | To be terminated into a JTAG connector. |
| 86 | JTAG_TDO | To be terminated into a JTAG connector. |
| 87 | JTAG_TMS | To be terminated into a JTAG connector. |
| 88 | JTAG_TCK | To be terminated into a JTAG connector. |
| 89 | JTAG_TDI | To be terminated into a JTAG connector. |

**Application circuit**

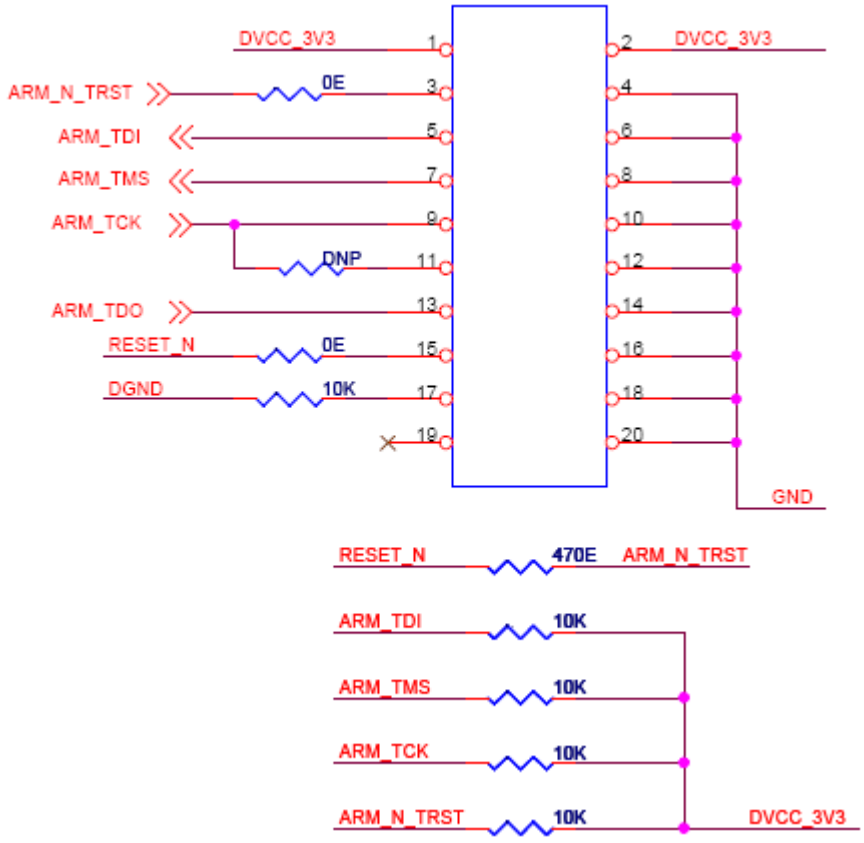



Figure 12: Application circuit for JTAG connector

## Peripherals

The Navika-111 supports several industry standard peripherals. These allow seamless connectivity either for Man-Machine interface or to interface additional embedded devices. The following peripherals are supported on the Navika-111.

- UART
- SPI
- TWI
- GPIO
- SPORT
- USB
- CAN
- Battery backed circuitry
- Time and frequency outputs
- ADC
- Frequency Counter

**UART**

The Navika-111 provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UART. The UART port provides a full UART interface (with hardware flow-control) to other peripherals or hosts, supporting full duplex, DMA-supported, asynchronous transfers of serial data. The UART supports five to eight data bits, one or two stop bits, and no, even, or odd parity.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 50 | UART1_RXD | To be connected to the Transmit line of the host processor.<br><br>It is possible to bring out the UART lines through a RS-232 line driver into a standard D-type connector. A typical circuit is shown below. |
| 51 | UART1_TXD | To be connected to the Receive line of the host processor.<br><br>It is possible to bring out the UART lines through a RS-232 line driver into a standard D-type connector. A typical circuit is shown below. |
| 52 | UART1_CTS | To be connected to the CTS line of the host processor. To be left unconnected if flow control is not required. |
| 53 | UART1_RTS | To be connected to the RTS line of the host processor. To be left unconnected if flow control is not required. |

The UART port supports following two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory.

The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

**Application Circuit**

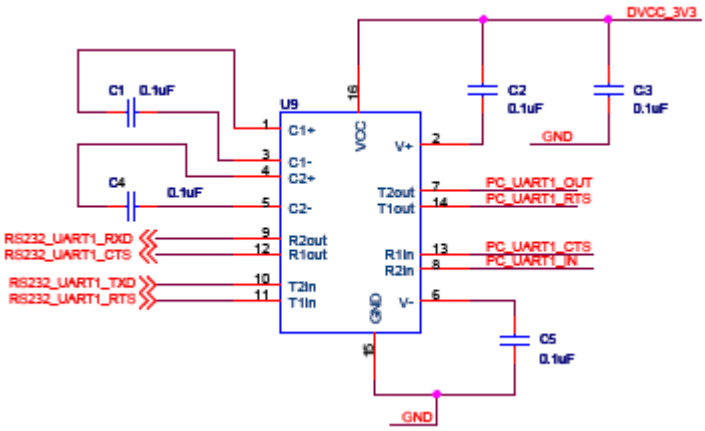



Figure 13: Application circuit for RS-232 level translation

**SPI**

The serial peripheral interface (SPI) is an industry standard synchronous serial link that will help in communicating with multiple SPI-compatible devices.
SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full duplex, synchronous serial interface, which supports both master and slave modes and can operate in a multi-master environment. This peripheral implementation includes programmable baud rates, clock phase and clock polarity. The Serial Peripheral Interface is essentially a shift register that serially transmits and receives data bits to/from other SPI ports. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 7 | SPI_CS | To be connected to the Slave Select line of the host processor. Here, the SPI port of the Navika-111 acts as a slave. |
| 8 | MISO | To be connected to the MISO line of the host processor. |
| 9 | SPI_CLK | To be connected to the SPI clock line of the host processor or serial flash. |
| 10 | MOSI | To be connected to the MOSI line of the host processor. |
| 13 | SPI_FLASH_CS | To be connected to the Chip Select line of a serial flash. To be used when Boot_mode [ ] = '01'. |
| 70, 71, 72, 73, 74, 75, 76 | GPIO 2 to 7 | To be used as SPI Slave select lines when the SPI port of Navika-111 is the master. |

The SPI block is configured in SLAVE mode by default (after reset). The major applications of SPI in Navika-111 are –

- Load the boot image by an external host when external boot option is selected.
- As a serial interface for data transfer

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin (SPISS) lets other SPI devices select the processor. Using these pins, the SPI port provides a full duplex, synchronous serial interface, which supports both master/slave modes and multi-master environments.

The SPI port's clock rate is calculated as:

*SPI Clock Rate = FSCLK / 2 x SPI Baud*

Where, the 16-bit SPI_Baud register contains a value in the range from 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

**TWI**

The Navika-111 includes a two-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I2C® bus standard. The TWI module offers the capabilities of master and slave operation support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 57 | TWI_SCL | To be connected to the I2C clock line of the host processor. |
| 58 | TWI_DATA | To be connected to the I2C data line of the host processor. |

The default Master/Slave address is 0x00.

**GPIO**

The Navika-111 provides 8 bi-directional, general purpose I/O (GPIO) pins. Each general-purpose port pin can be individually controlled as either input or output. The default status of all GPIO pins upon reset is input.

The same GPIO lines also double up as SPI slave select lines when in SPI communication mode.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 70 | GPIO2 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 71 | GPIO3 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 72 | GPIO4 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 73 | GPIO5 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 74 | GPIO6 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 75 | GPIO7 | Can be used as an I/O or as a SPI Slave Select.<br>Supports external interrupts when used as an I/O. |
| 76 | GPIO1 | Can be used as an I/O.<br>Supports external interrupts. |
| 77 | GPIO0 | Can be used as an I/O.<br>Supports external interrupts. |

**SPORT**

The Navika-111 incorporates one dual-channel synchronous serial port for serial and multiprocessor communications.

The SPORT supports the following features:

- I2S capable operation
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I2S stereo audio
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (fSCLK/131,070) Hz to (fSCLK/2) Hz
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most significant bit first or least significant bit first
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync

- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA
- ·Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 27 | SPORT_YADATA | Can be connected to the data line of the I2S port of the host processor. |
| 28 | SPORT_YCLK | Can be connected to the clock. |
| 29 | SPORT_YFS | Can be connected to the frame synch signal on the host processor. For internal frame synch generation, this line can be left open. |
| 30 | SPORT_YBDATA | Can be connected to the data line of the I2S port of the host processor. |
| 36 | SPORT_XFS | Can be connected to the frame synch signal on the host processor. For internal frame synch generation, this line can be left open. |
| 37 | SPORT_XCLK | Can be connected to the clock. |
| 38 | SPORT_XBDATA | Can be connected to the data line of the I2S port of the host processor. |
| 39 | SPORT_XADATA | Can be connected to the data line of the I2S port of the host processor. |

**USB**

The Navika-111 provides a full speed USB 2.0 controller to support direct connection to a host system at 12M bits per second data rate. The interface provides a flexible programmable environment with up to seven data end points and one control endpoint. Each endpoint can support all of the USB data types and packet sizes including control, bulk, interrupt, and isochronous. The USB interface on the Navika-111 is an alternative to the UART's for data transfer.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 45 | USB_DM | Can be connected to the Data – (DM) line of the host processor. |
| 46 | USB_DP | Can be connected to the Data + (DP) line of the host processor. |
| 48 | USB_CID | Reserved. |
| 49 | USB_VBUS | Power supply for USB PHY. To be connected to DVCC_3V3 |

## CAN

The interface to the CAN bus on the Navika-111 is a simple two-wire line - input Rx pin and an output Tx pin. Both pins operate at TTL level and are appropriate for the operation with CAN bus transceivers according to ISO/DIS 11898 (e. g. Texas Instruments SN65HVD230D, Philips PCA 82C250, Bosch CF150 or Siliconix SI 9200) or with a modified RS-485 interface.

In the standard implementation, 3 acceptance mask registers and 16 mailboxes are implemented.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 55 | CAN_TX | Can be connected to the CAN bus through a CAN transceiver as shown in the below application circuit. |
| 56 | CAN_RX | Can be connected to the CAN bus through a CAN transceiver as shown in the below application circuit. |

### Application circuit

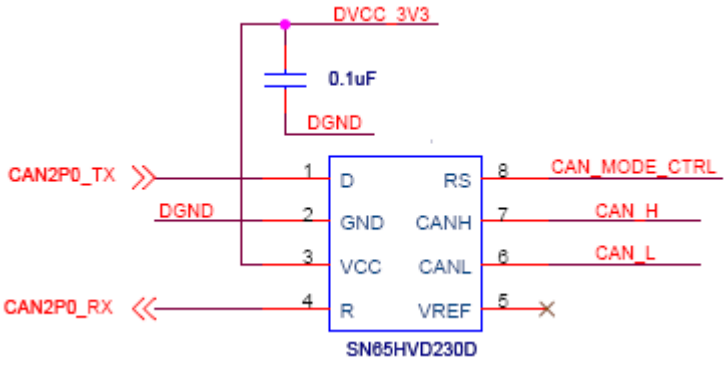



Figure 14: Application circuit for CAN bus interface

### Battery backed circuitry

The Navika-111 has several peripherals that are capable of operating on battery power. These are listed below –

- Battery-Backed Counter (BBC): This is a 32-bit counter provided as part of the GPS baseband. It runs on battery domain and maintains the counter over power cycles. The value from the counter is used to assist the hot and warm start modes of the GPS.
- Battery-Backed SRAM (BBSRAM): This is a 32Kbit memory space and is used to hold the GPS parameters such as Ephemeris, Almanac, Position and Time estimates to facilitate hot and warm start modes.
- Real Time Clock (RTC): The RTC is part of the ARM sub-system

**Time and Frequency Outputs**

The Navika-111 provides a one pulse per second (1PPS) output from the GPS section. This pulse is crucial for several timing applications. To obtain this pulse output, it is necessary that the GPS firmware supports the generation of this pulse.

In addition, the Navika-111 provides 3 programmable clock outputs which allow generation of various clock frequencies (CMOS, square wave) based on the processor internal clock or an externally supplied clock.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 60 | CLKOUT3 | Uses the processor 90.024MHz clock. Divider values of 2 to 31 can be used to derive the clock output |
| 61 | CLKOUT2 | Uses the processor 90.024MHz clock. Divider values of 2 to 31 can be used to derive the clock output |
| 64 | CLKOUT1 | Uses the processor 90.024MHz clock. Divider values of 2 to 31 can be used to derive the clock output |
| 65 | PTTI | To be connected to an I/O pin of the host processor or taken out (through a buffer) to a connector. |

**ADC**

Navika-111 supports an 10-bit Analog to Digital converter which can be used to measure the analog input.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 5 | ADC_IN | Input voltage range should be between 0 and 2.8V. Sampling rate is a maximum of 1.0833MHz with a precision of 10mV to 20mV. |

In order to ensure that the voltage input to the ADC_IN pad is within the range specified, it is important to first understand the voltage range of the sensor which is supposed to be monitored. A simple resistor voltage divider can then be designed to ensure that the voltage is scaled down.

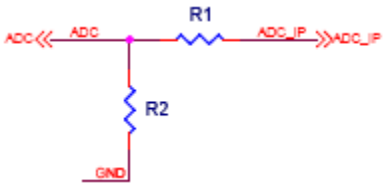



*Figure 15: ADC input level translation*

### Frequency Counter

Navika-111 supports a frequency counter which allows an external clock (for eg. pulses from a vehicle odometer) to be fed directly to the module. It is necessary to condition the signal before feeding it to the EXT_TIMCLK pad of the module.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 68 | EXT_TIMCLK | Can be used to feed external clocks on this pin at 0 to 3.3V, with 40% to 60% duty cycle |

## Power Supply

Navika-111 operates out of a single supply. However, there are a few more pads that have to be addressed when designing the power supply circuit for the Navika-111. The below table describes the different pads associated with the Power Supply domain of the Navika-111.

| Pin identification | Signal / Power name | Connection Detail |
|---|---|---|
| 1, 2 | DVCC_4V0 | 4.0V, 2.5A (max).<br>Range of input voltage can be from 3.4V to 4.4V.<br>This is the overall supply to the Navika-111 module. |
| 4 | GSM_DVCC_4V0 | As the GSM modem requires a larger capacitance to ensure reliable operation, the GSM_DVCC_4V0 pad is provided to allow the provision of mounting additional capacitance to the GSM modem of the Navika-111. Typical value of capacitance is 470uF (with a low ESR of less than 1 Ohm). A higher value will be preferred. The capacitor should be placed as close as possible to the pad. |
| 26 | DVCC_2V8 | This is the 2.8V power supply derived from the DVCC_4V0 input of the Navika-111 module. It is brought out of the Navika-111 module and can be used to drive loads of upto 50mA |
| 31 | VBAT_3V0 | 3.0V, 20uA.<br>This is the supply to the battery backed domain of the Navika-111 module. |
| 40 | DVCC_3V3 | This is the 3.3V power supply derived from the DVCC_4V0 input on the Navika-111 module. It is brought out of the Navika-111 module and can be used to drive loads of upto 200mA. |

# Chapter 3: Specifications

This chapter lists the specifications of the Navika-111 module. The performance, electrical and environmental specifications are listed in this chapter.

## *Functional Specification*

### GPS Specifications

| Parameter | Specification |
|---|---|
| **General** | |
| Channels | 32<br>16 Acquisition, 16 Tracking |
| Signals supported | GPS L1 C/A<br>SBAS (WAAS, EGNOS, GAGAN, MSAS) |
| **Sensitivity (as referenced to the output of a GPS simulator)** | |
| Acquisition Sensitivity<br>(with active antenna with noise temperature of 100K) | -158 dBm (Hot start, 1SV @<br>-143 dBm)<br>-148 dBm (Cold start)<br>-160 dBm (Reacquisition) |
| Tracking Sensitivity<br>(with active antenna with noise temperature of 100K) | -162 dBm |
| **TTFF** | |
| Hot Start TTFF<br>(with valid ephemeris, almanac, position and time estimate) | 1 sec (typical) switch OFF/ON cycle less than 1 hour |
| Warm Start TTFF<br>(with almanac, position and time estimate) | 30 sec (typical) |
| Cold Start TTFF<br>(without almanac, time, or position) | 35 sec (typical) |
| **Accuracy** | |
| Position Accuracy<br>(Open sky, C/N0 of 40dB-Hz or higher, HDOP < 2, VDOP < 3) | 2.5 m (CEP, without SBAS)<br>2.0 m (CEP, with SBAS) |
| Velocity Accuracy | Speed: 0.1 m/sec (RMS)<br>Heading: 0.5 degrees |
| 1PPS Accuracy<br>(Open sky, C/N0 of 40dB-Hz or higher, HDOP < 2, VDOP < 3) | 25ns (RMS) |
| **Dynamics** | |
| Dynamics | Velocity: 515 m/s<br>Acceleration: 4g |

| | |
|---|---|
| | Jerk: 7 $m/s^3$ |
| Altitude | 18000 m |
| **GPS Data output** | |
| Position Update Rate | 1Hz |

Table 3: Functional specifications of the GPS running on the Navika-111

## GSM/GPRS Specifications

| **Parameter** | **Specification** |
|---|---|
| Bands supported | Quad band 850/900/1800/1900 MHz |
| GSM | Compliant to GSM phase 2/2+<br>- Class 4 (2W @ 850/900MHz)<br>- Class 1 (1W @ 1800/1900MHz) |
| GPRS | Multi-slot class 12/10, max 85.6Kbps (downlink/uplink)<br>Mobile station class B<br>PBCCH support<br>Coding schemes CS 1, 2, 3, 4<br>PPP-stack<br>CSD upto 14.4 Kbps<br>USSD<br>Non-transparent mode |
| SMS | Point to point MO and MT<br>SMS cell broadcast<br>Text and PDU mode |
| Software features | 0710 MUX protocol<br>Embedded TCP/UDP protocol<br>FTP/HTTP<br>MMS<br>E-mail<br>DTMF<br>Jamming detection<br>Audio record<br>TTS |
| Voice features | Tricodec<br>- Half rate (HR)<br>- Full rate (FR)<br>- Enhanced Full rate (EFR)<br>AMR<br>- Half rate (HR)<br>- Full rate (FR)<br>Hands free operation |

## Bluetooth Specifications

| Parameter | Specification |
|---|---|
| Compliance | Bluetooth Specification 3.0+ EDR |
| RF | - -95 dBm with interference rejection<br>- Hardware AGC |
| Baseband | - Upto 4 simultaneous active ACL links<br>- Upto 1 simultaneous SCO or eSCO link with CVSD coding<br>- Scatternet support (upto 4 piconets)<br>- Supports sniff mode<br>- Idle mode and sleep mode for ultra-low power consumption<br>- Channel quality driven data rate adaption |
| Platform | - Embedded processor for Bluetooth protocol stack with in-built memory system<br>- Fully verified ROM based system with code patch for feature enhancement |

## FM Specifications

| Parameter | Specification |
|---|---|
| Frequency bands supported | 76 – 108MHz worldwide FM bands |
| Tuning step | 50KHz |
| RDS/RBDS | Supported |
| Other features | - Superior stereo noise reduction<br>- Soft mute volume control<br>- Supports short antenna, auto calibration for different FM channels |

## *Electrical Specifications*

### Absolute Maximum Ratings

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the module. This is a stress rating only; functional operation of the module at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

| **Parameter** | **Rating** |
|---|---|
| DVCC_4V0 (Mains Power Supply) | 4.5 V |
| VBAT_3V0 (Backup Power Supply) | 3.6 V |
| USB_VBUS (USB Power Supply) | 3.6 V |
| Peripheral Input pins | 3.6 V |
| Current | 2.2 A |
| Load capacitance | 20pF |
| Power at GPS_ANT_IN | -5 dBm (continuous wave) |
| Storage temperature | -40 C to +85 C |
| Operating temperature | -40 C to +85 C |

Table 4: Absolute maximum ratings of the Navika-111

## Operating Conditions

- The operating conditions are stated for an ambient temperature of 25 C

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DVCC_4V0 | | 3.4 | 4.0 | 4.4 | V |
| VBAT_3V0 | | 2.3 | 3.0 | 3.3 | V |
| SIM_VDD | | | 3.0<br>1.8 | | V |
| USB_VBUS | | 3.0 | 3.2 | 3.3 | V |
| USB_IO | | 3.0 | 3.2 | 3.3 | V |
| $V_{IH}$ | All peripheral pins except ADC, PWM | 1.6 | | 2.8 | V |
| $V_{IL}$ | All peripheral pins except ADC, PWM | -0.3 | | 0.7 | V |
| $V_{OH}$ | All peripheral pins except ADC, PWM | 1.7 | 1.8 | | V |
| $V_{OL}$ | All peripheral pins except ADC, PWM | | 0.2 | 0.7 | V |
| $V_{IH}$ | ADC, PWM | 2.1 | | 3.1 | V |
| $V_{IL}$ | ADC, PWM | -0.3 | | 0.7 | V |
| $V_{OH}$ | ADC, PWM | 2.4 | | | V |
| $V_{OL}$ | ADC, PWM | | | 0.4 | V |
| $V_{IH}$ | SIM interface pins | 1.4 | | | V |
| $V_{IL}$ | SIM interface pins | 2.4 | | | V |
| $V_{OH}$ | SIM interface pins | | | 0.27<br>0.4 | V |
| $V_{OL}$ | SIM interface pins | 1.62<br>2.7 | | | V |
| Tj | | -40 | 25 | 125 | C |
| $I_{OH}$ @ $V_{OH}$ = 1.7V | All peripheral pins except ADC, PWM | 7.5 | 12.3 | 18.2 | mA |
| $I_{OH}$ @ $V_{OL}$ = 0.7V | All peripheral pins except ADC, PWM | 5.8 | 9.3 | 12.9 | mA |
| $I_{IH}$ | SIM interface pins | -1 | | 1 | uA |
| $I_{IL}$ | SIM interface pins | -1 | | 1 | uA |
| $I_{VCC}$ @ 3.3 V | | | | 100 | mA |
| $I_{VBCKUP}$ @ 3.0 V | | | 20 | | uA |
| $I_{SIM}$ | SIM card | | | 10 | mA |
| Input capacitance | | | 10 | | pF |
| Output Capacitance | | | 20 | | pF |

Table 5: Operating conditions of Navika-111

## *Environmental Specifications*

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | | -40 | 25 | +85 | $^0$C |
| Storage Temperature | | -40 | 25 | +85 | $^0$C |

Table 6: Environmental Specifications of Navika-111

# Chapter 4: Assembly Instructions

## *Packaging and Shipment*

Navika-111 are packed in hermetically sealed reels to enable machine assembly and shipped in Tape and Reel format.

## *Storage*

As Navika-111 modules are moisture sensitive, appropriate precaution during assembly should be taken.

## *Handling*

Navika-111 module contains components that are ESD sensitive and require special care when handling. Below are a few precautions that will have to be exercised to ensure ESD protection.

- Use ESD-safe equipment for mounting where applicable (such as ESD safe soldering iron etc.)
- The GPS RF input port is ESD sensitive. It should be ensured that any connection being implemented for the antenna port (such as RF connector or passive patch antenna) should be done under ESD protected environment

## *Soldering*

Reflow soldering as per ROHS assembly profile is recommended for the Navika-111.

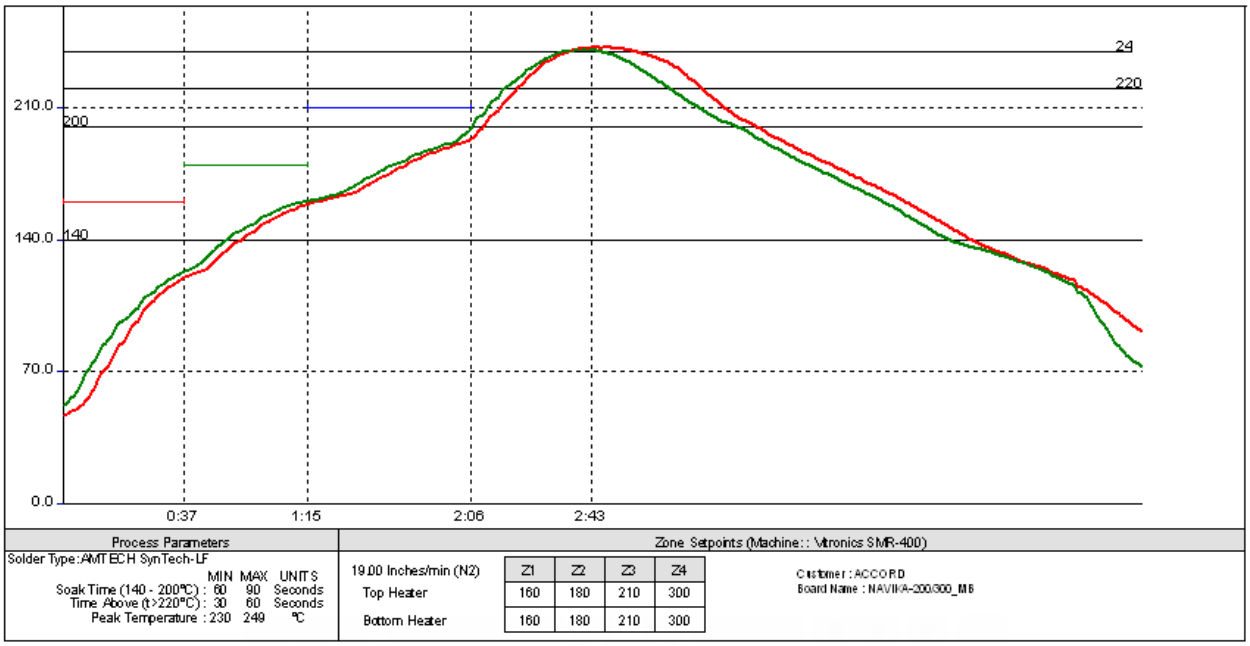



*Figure 16: Reflow profile for Navika-111*

## *Testing*

### GPS

Once assembled, the GPS functionality can be ascertained by connecting the signal from a GPS simulator to the RF connector input of the module.

A typical setup is shown below –

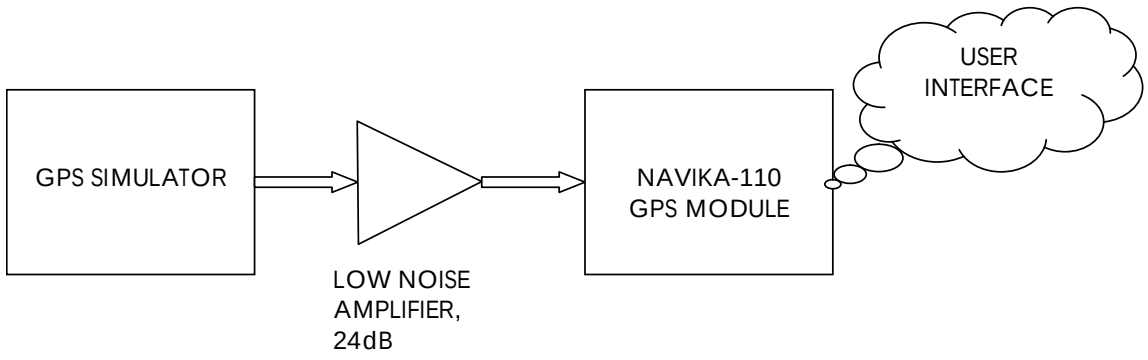



Figure 17: Typical test setup to validate GPS performance on the Navika-111

The output of the GPS Simulator is passed through a low noise amplifier and then on to the RF input of the Navika-111 module. The output of the Navika-111 can be connected to an user interface (PC application) and the C/N0 of the GPS satellite(s) can be evaluated against a reference value.

Typically, with a setting of -130dBm on the GPS simulator, the C/N0 of the satellite(s) should indicate about 40 dB-Hz.

# Chapter 5: Ordering Information

NAVIKA-111 can be ordered against the information mentioned below –

| Ordering part number | Description |
|---|---|
| NAVIKA-111 | GPS-GSM application module |
| NAVIKA-111-EVAL | Evaluation board of Navika-111 Contains Navika-111 module mounted on an evaluation PCB, USB cable, active GPS antenna and GUI installation CD |



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